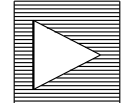


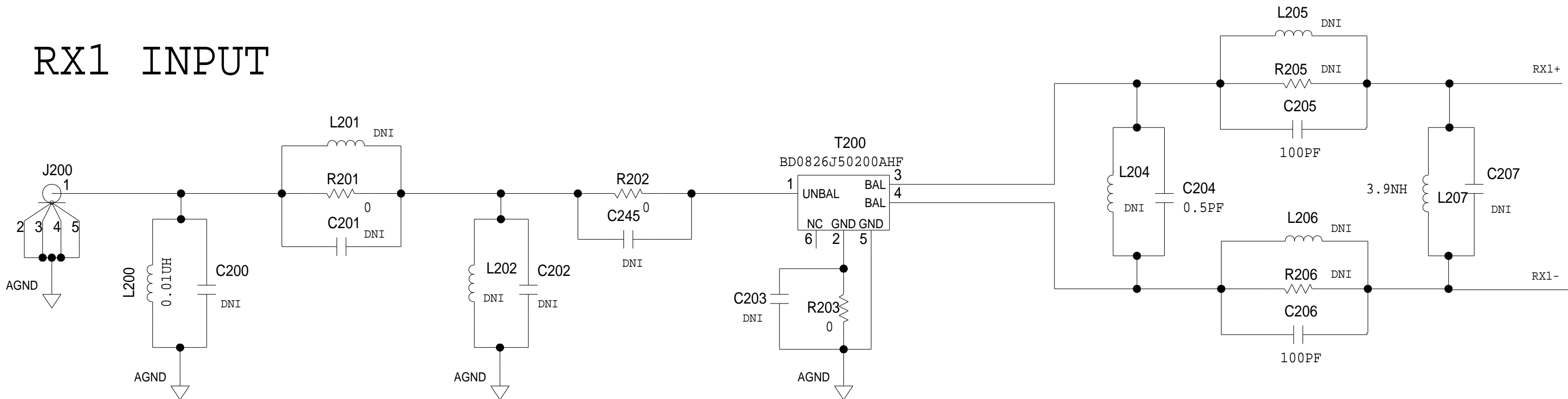
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	08JUN16	T KARPUS
B	AS PER ECR-066657	17JAN17	T KARPUS

TEMPLATE ENGINEER	DATE	SCHEMATIC				 ANALOG DEVICES			
HARDWARE SERVICES									
HARDWARE SYSTEMS									
TEST ENGINEER									
COMPONENT ENGINEER									
TEST PROCESS									
HARDWARE RELEASE		HW TYPE : Customer Evaluation Product(s): AD9371 PACKAGE : 196-lead 12X12_MM CBGA-family : Pitch-pitch StyleVendor Style							
DESIGNER J BOWNE	08JUN16	MASTER PROJECT TEMPLATE TBD		TESTER TEMPLATE no_template		DRAWING NO. 02_042572		REV. B	
PTD ENGINEER T KARPUS	08JUN16	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS X.XX +0.010 X.XXX +0.005 FRACTIONS +1/32 ANGLES +2				SIZE D	SCALE 1:1	CODE ID NO. CodeID	SHEET 1 OF 8

RF RX / ORX / SNIFFER INPUTS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

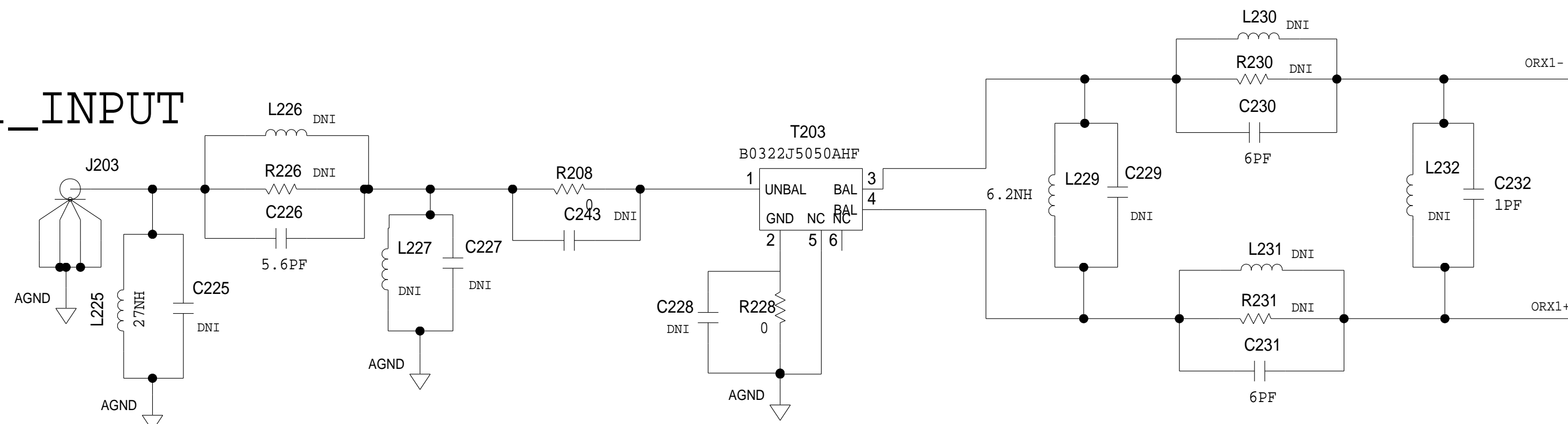
RX1 INPUT



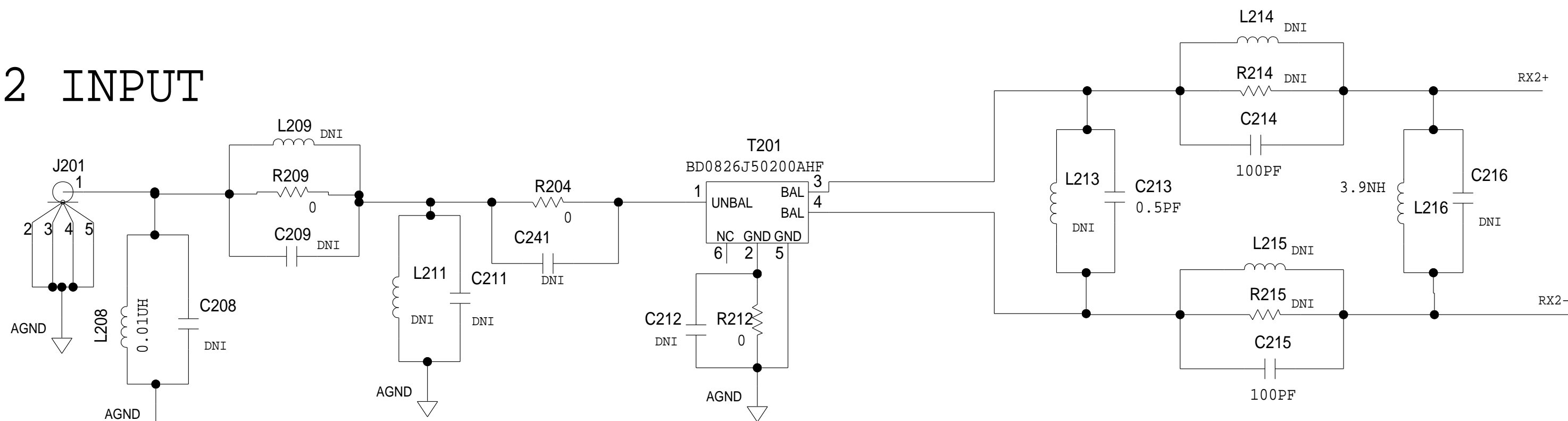
NOTE

EACH LC, RC OR RLC CLUSTER REPRESENTS A SINGLE PAD WHICH CAN BE POPULATED BY ONE OR NONE OF THE R,L OR C COMPONENTS.

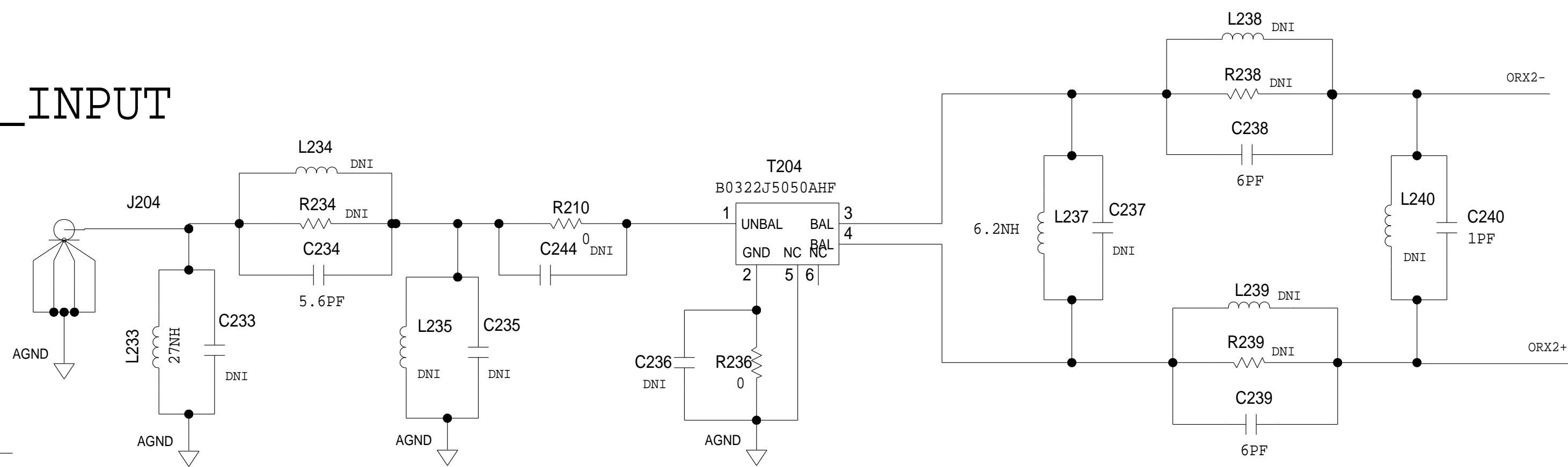
ORX1_INPUT



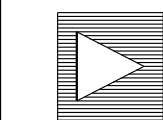
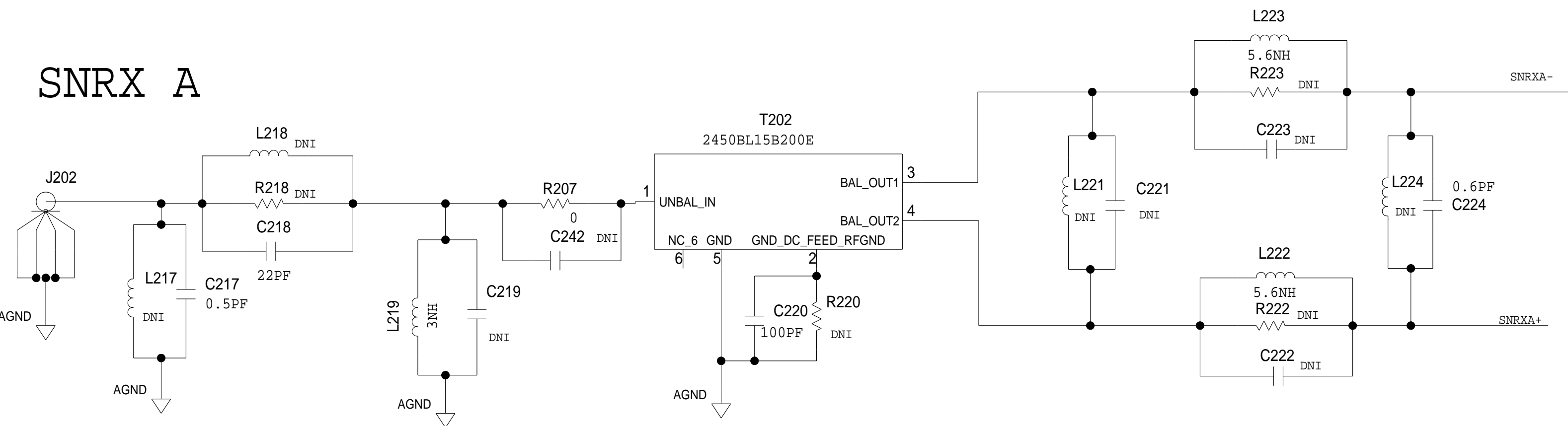
RX2 INPUT



ORX2_INPUT



SNRX A



ANALOG
DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD9371

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
T KARPUS

DRAWING NO.
02_042572

SIZE
D

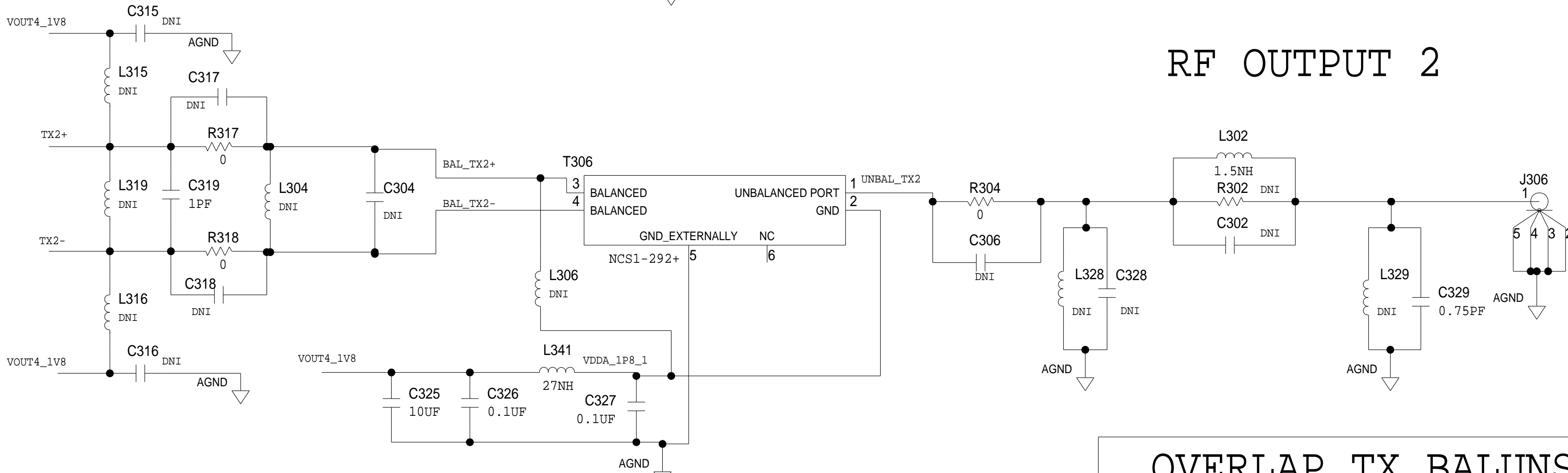
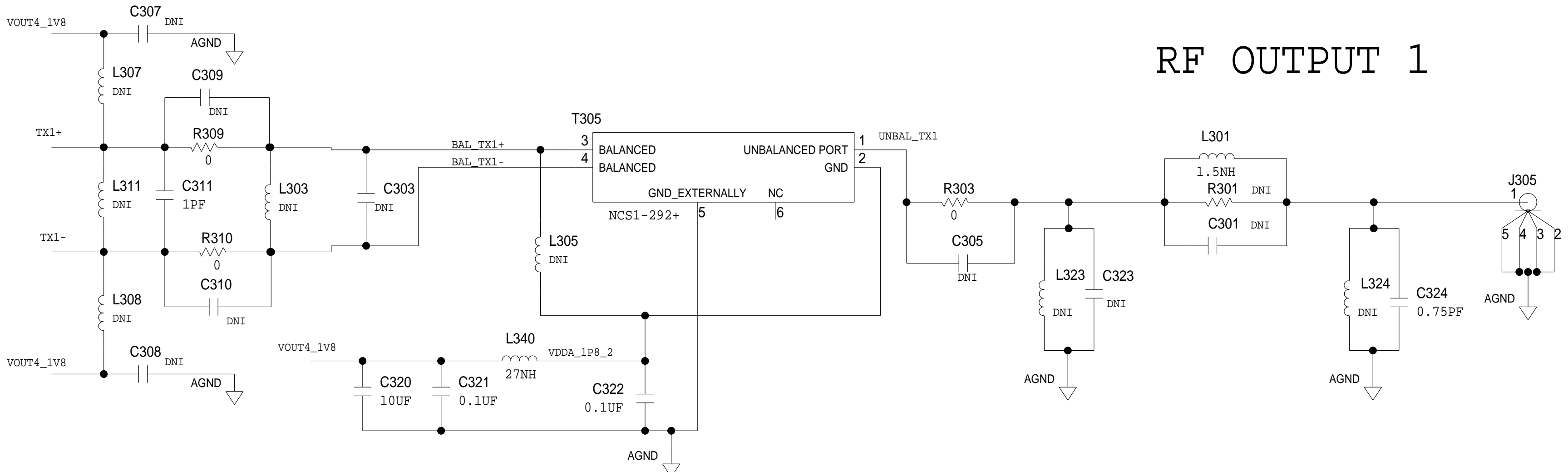
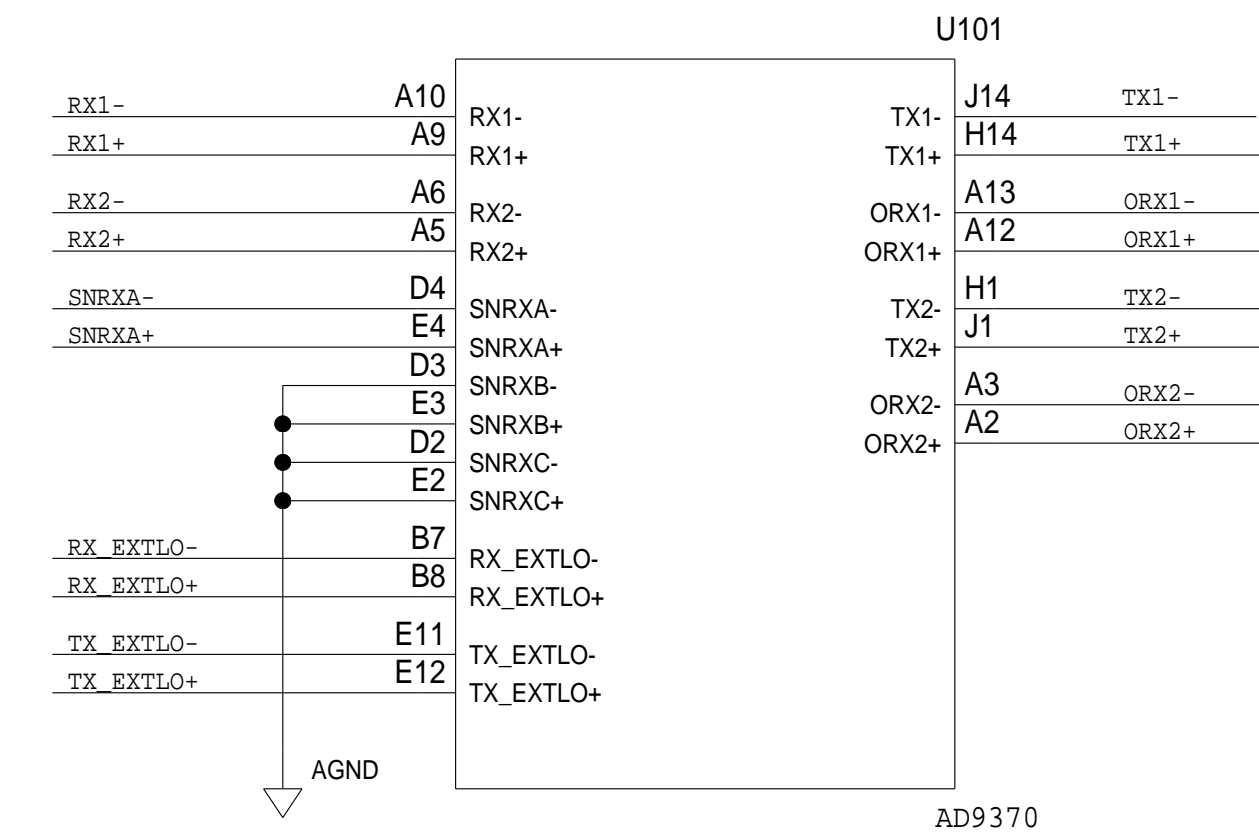
SCALE
1:1

SHEET 2 OF 8

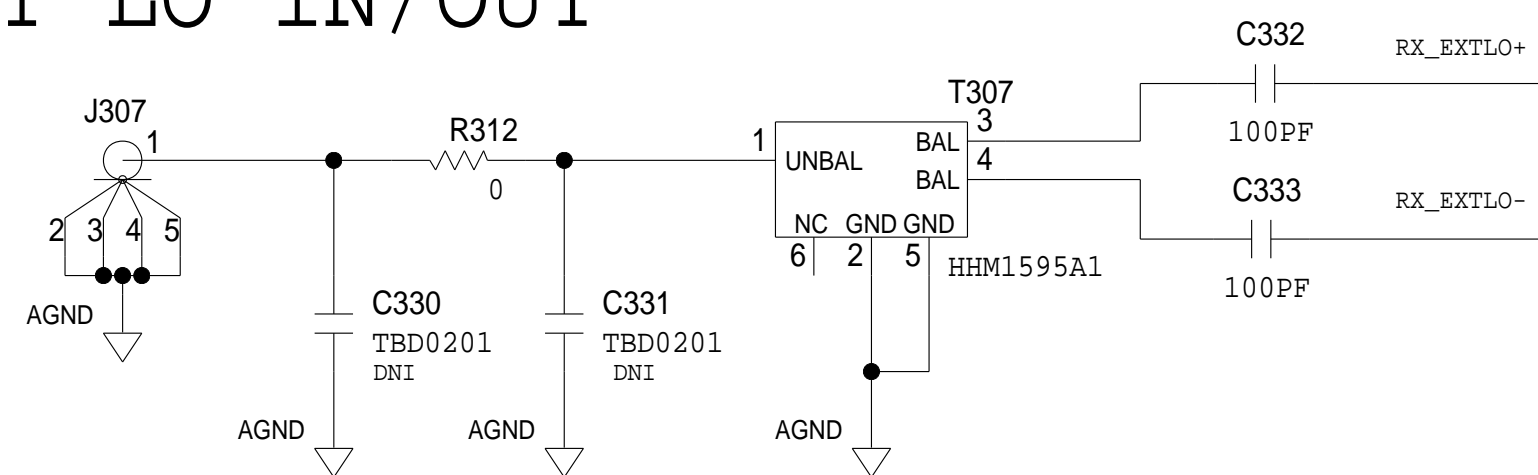
REV
B

RF TX OUT / EXT LO IN

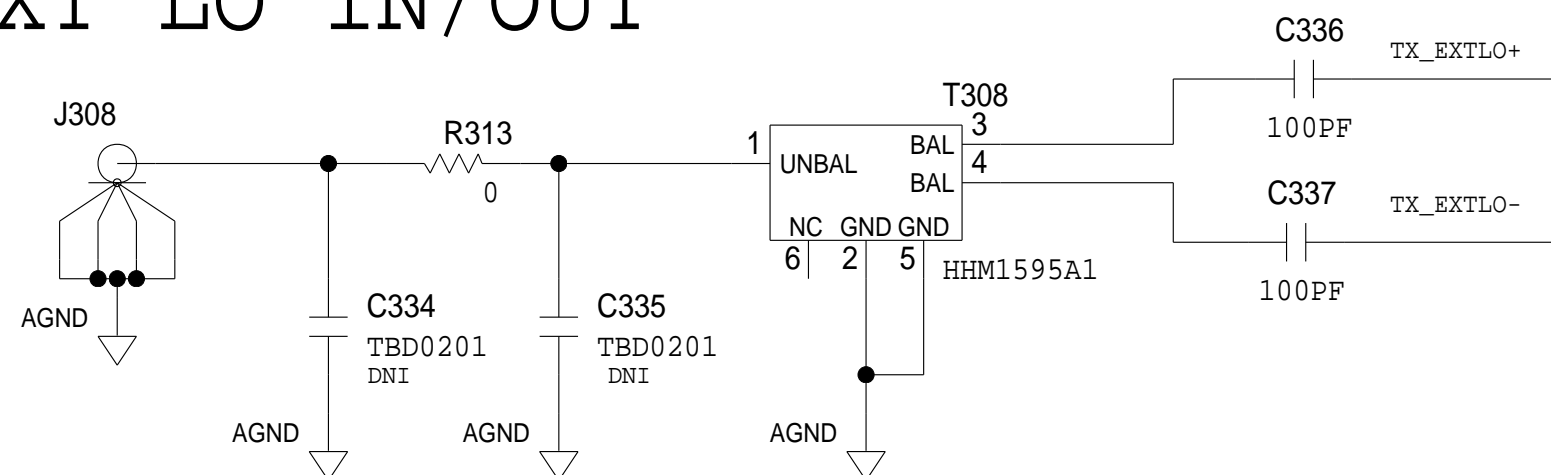
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



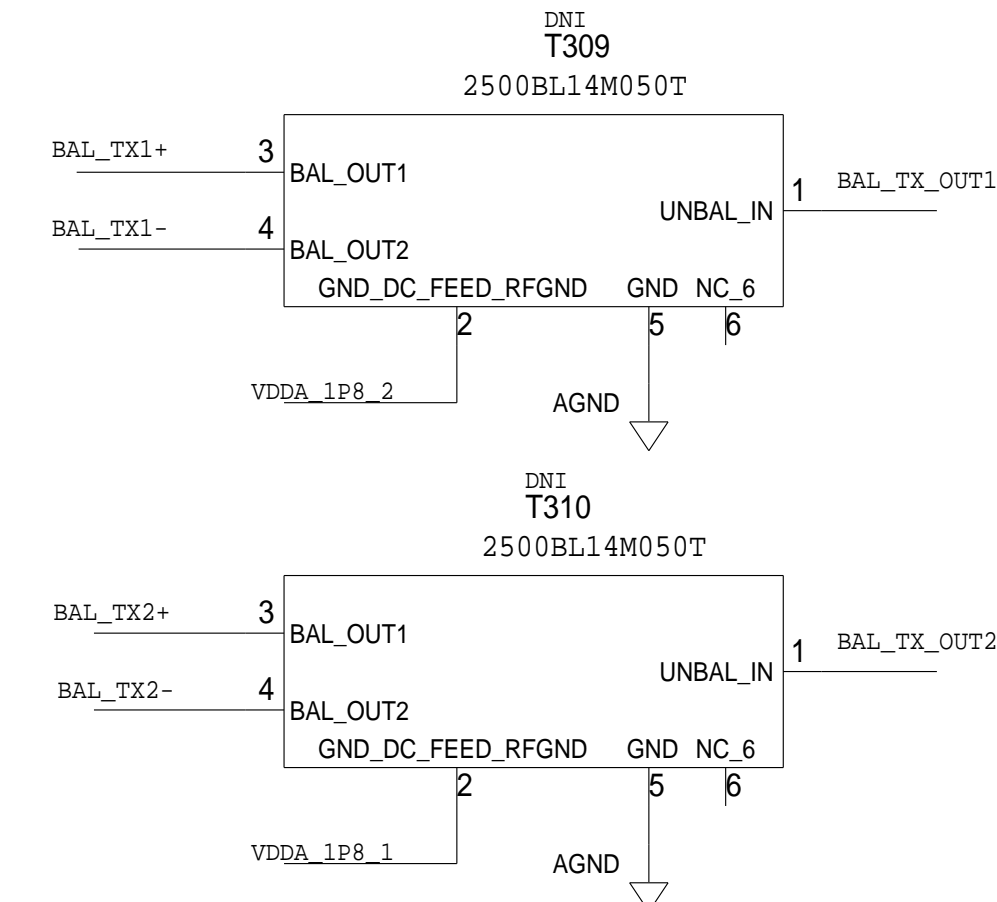
RX EXT LO IN/OUT



TX EXT LO IN/OUT



OVERLAP TX BALUNS

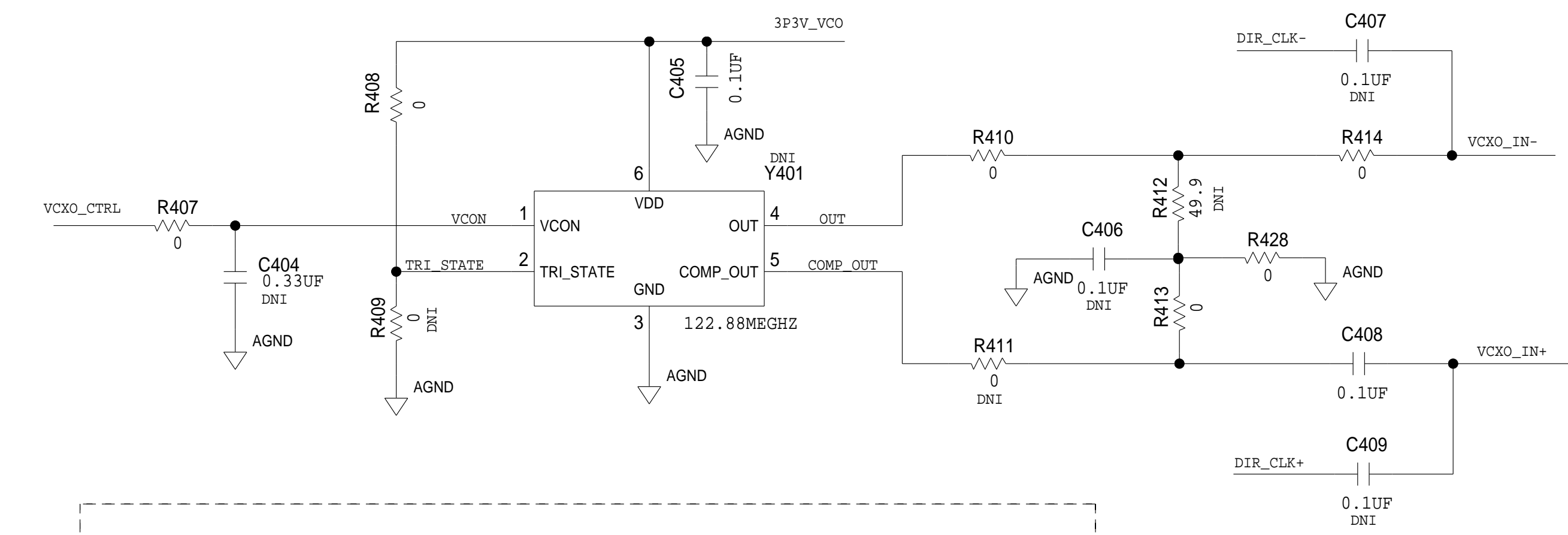
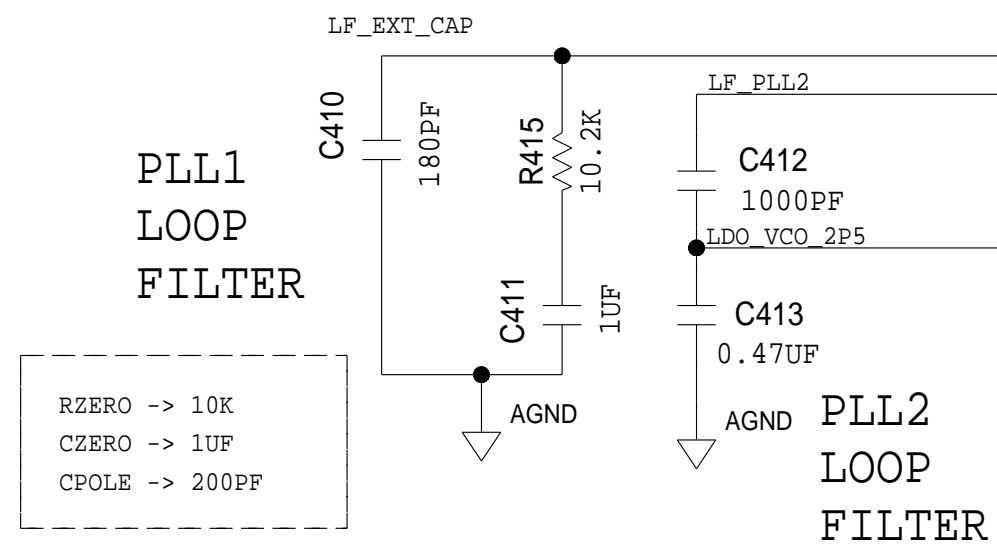
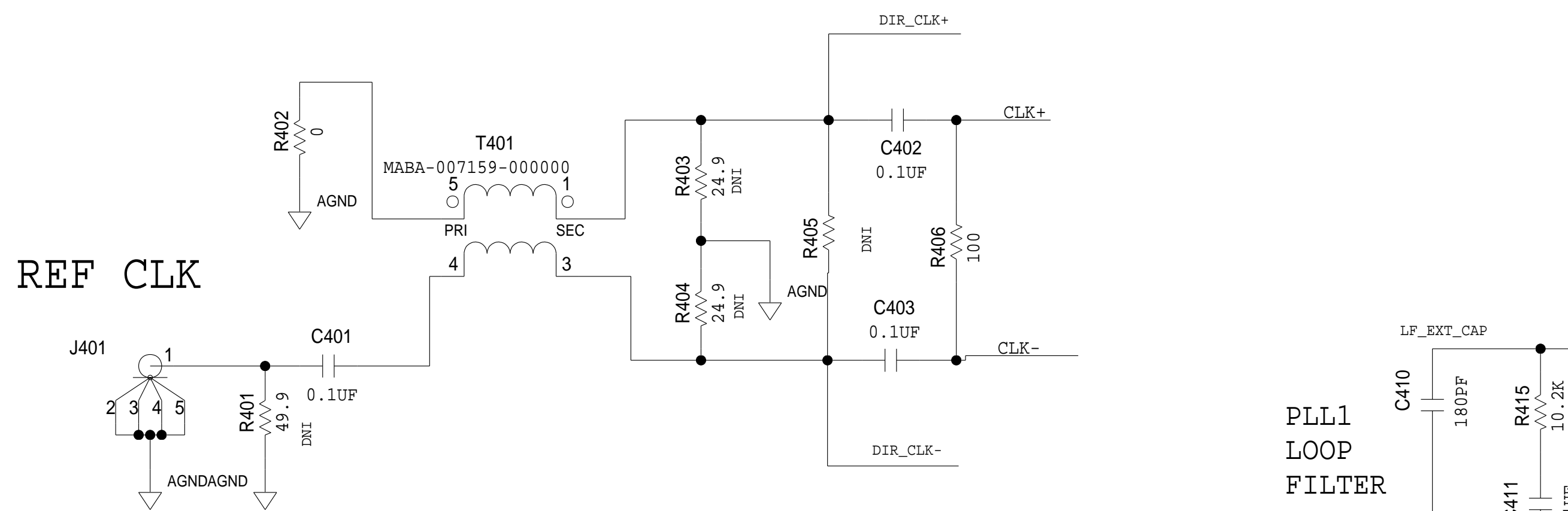


NOTE

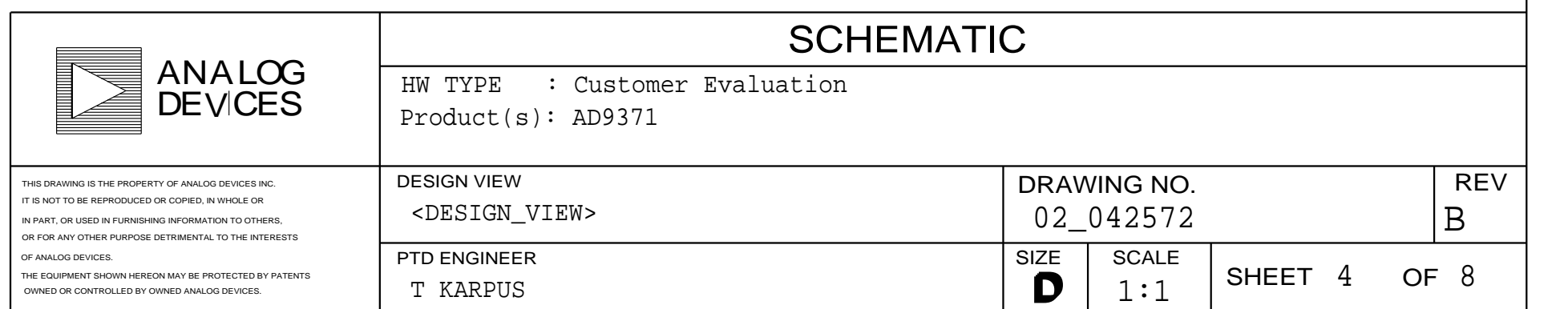
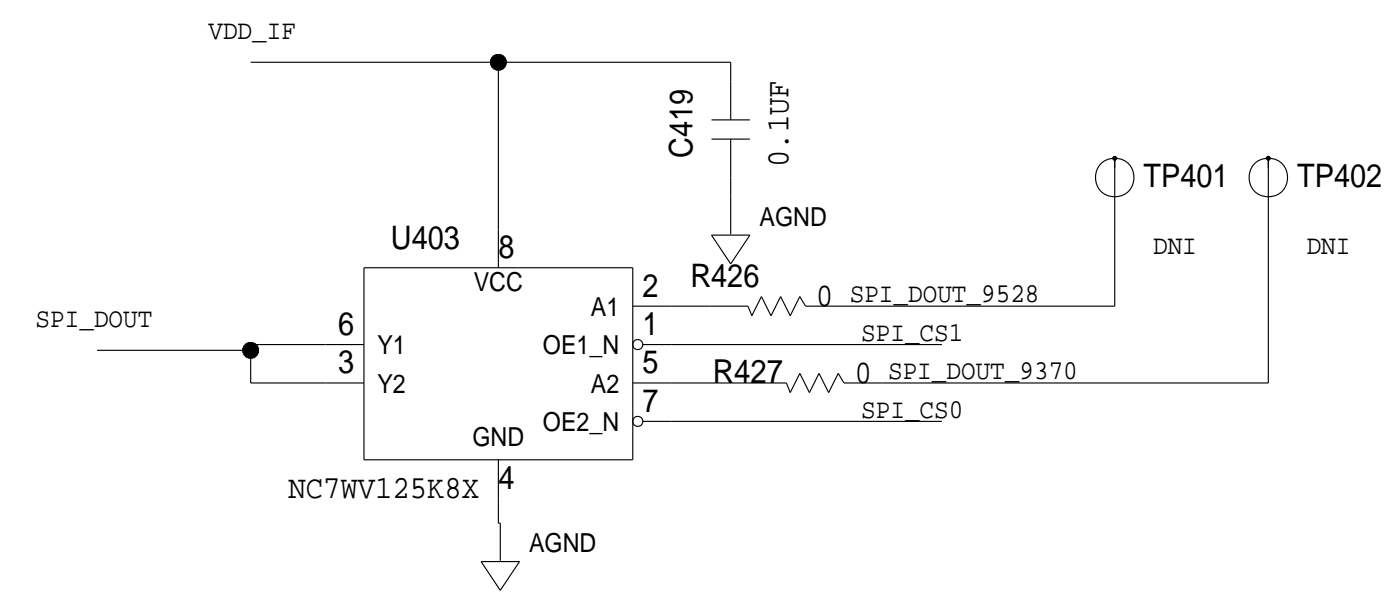
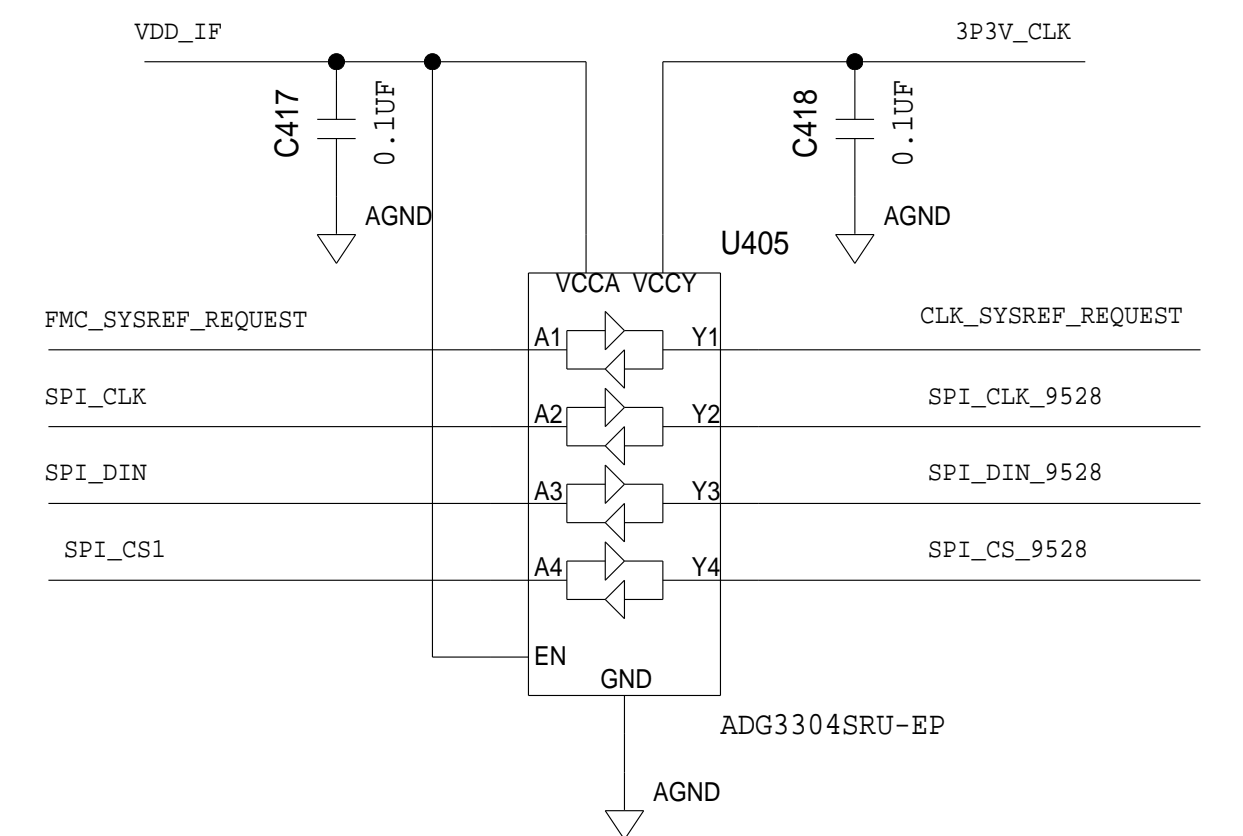
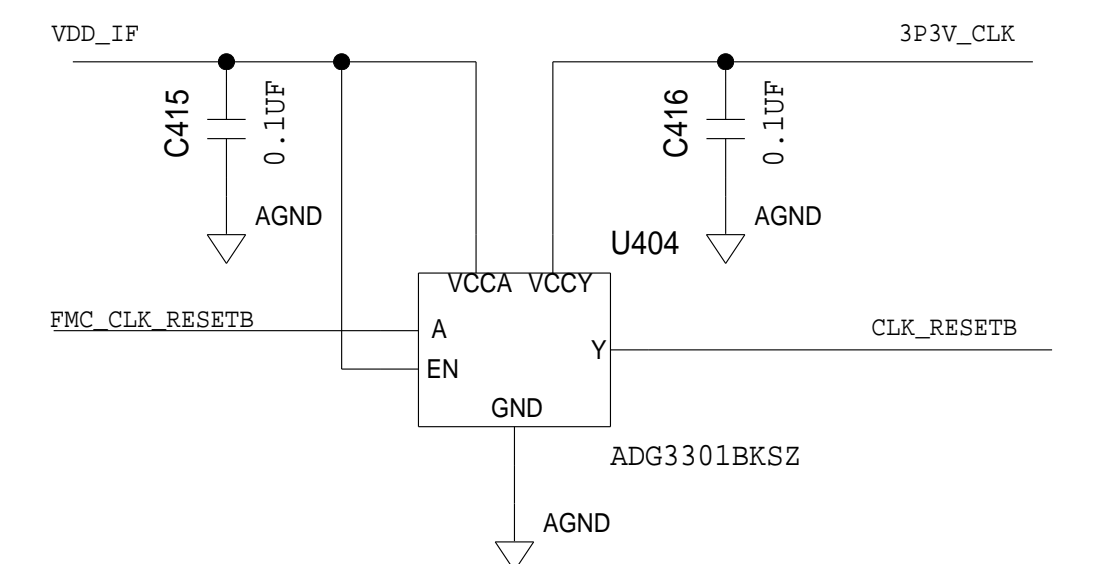
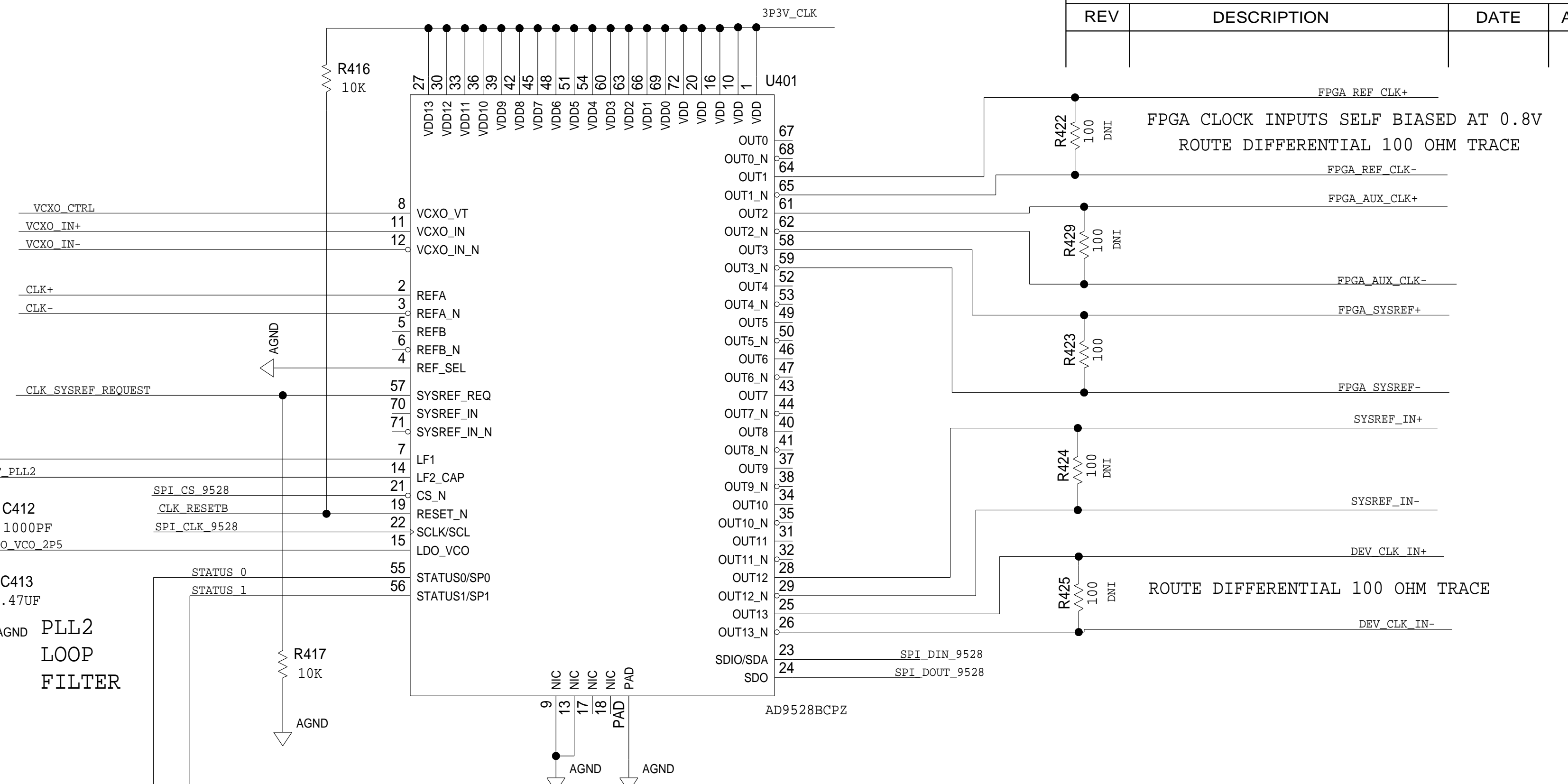
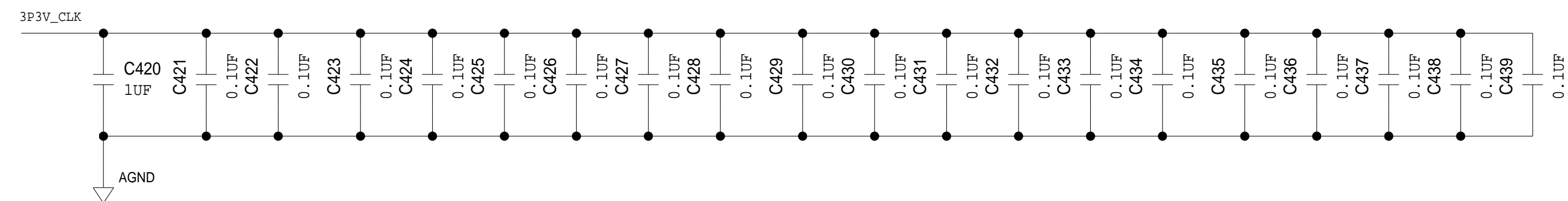
EACH LC OR RLC CLUSTER REPRESENTS A SINGLE PAD WHICH CAN BE POPULATED BY ONE OR NONE OF THE R,L OR C COMPONENTS.

SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042572		REV B
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 3 OF 8

CLOCK GENERATION



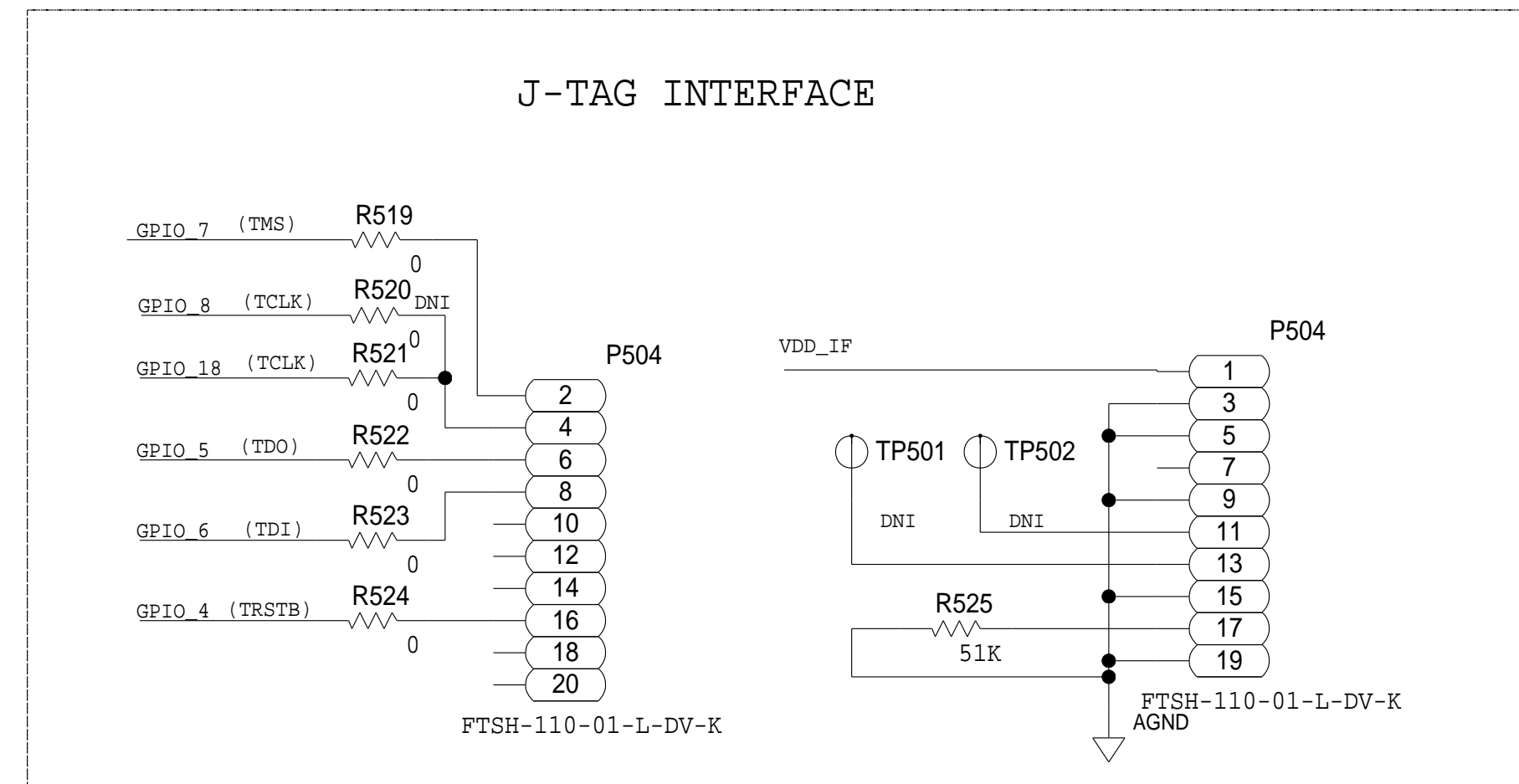
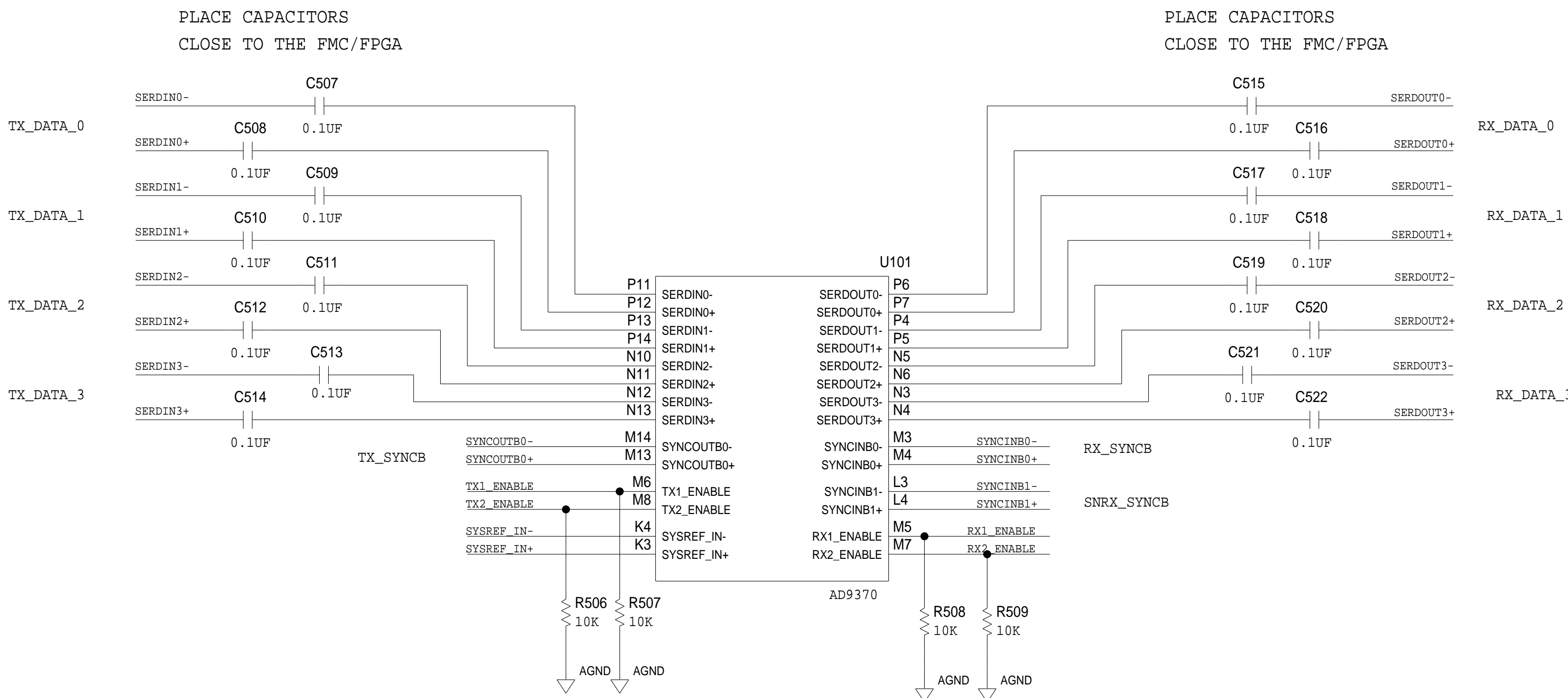
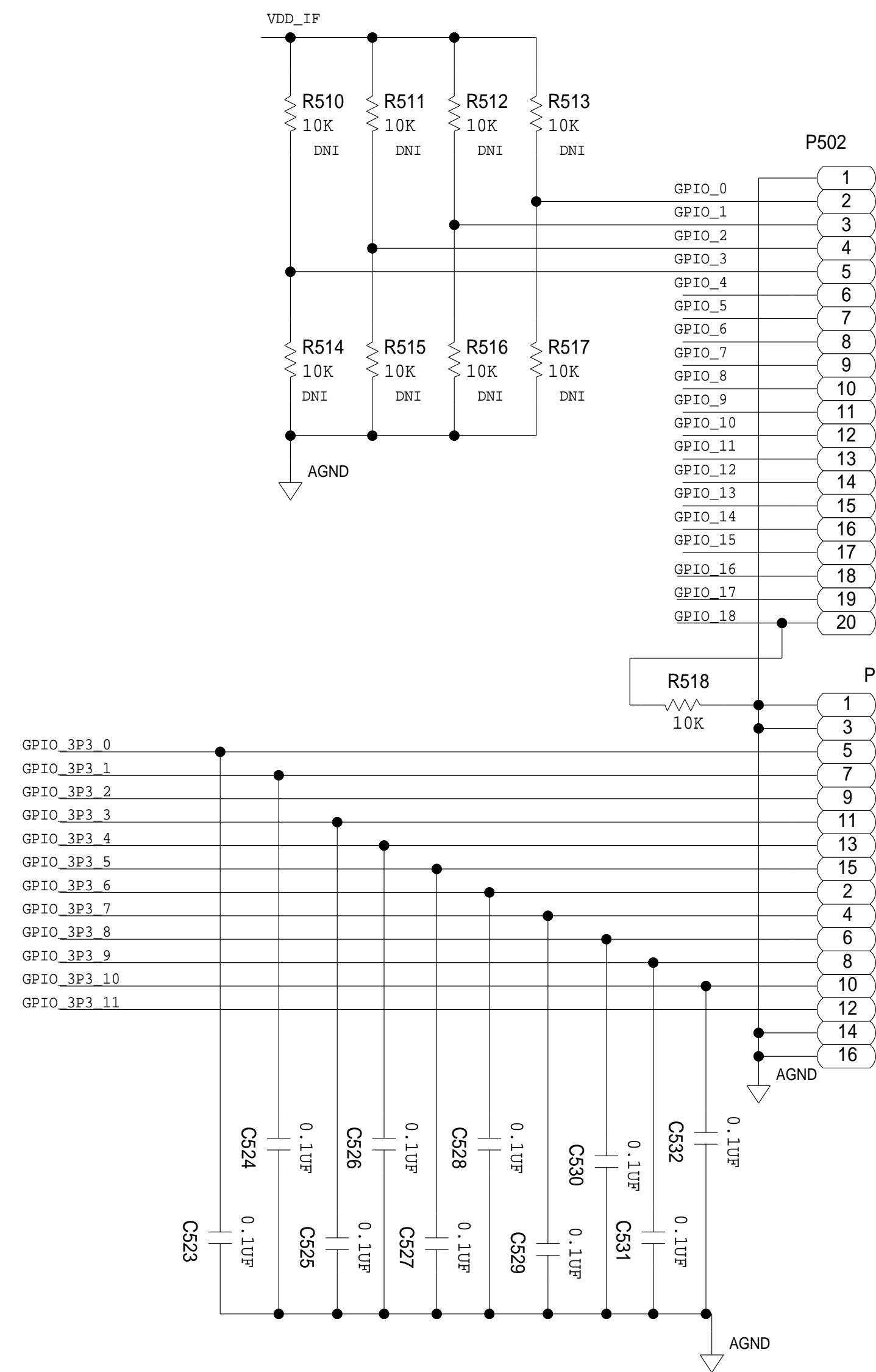
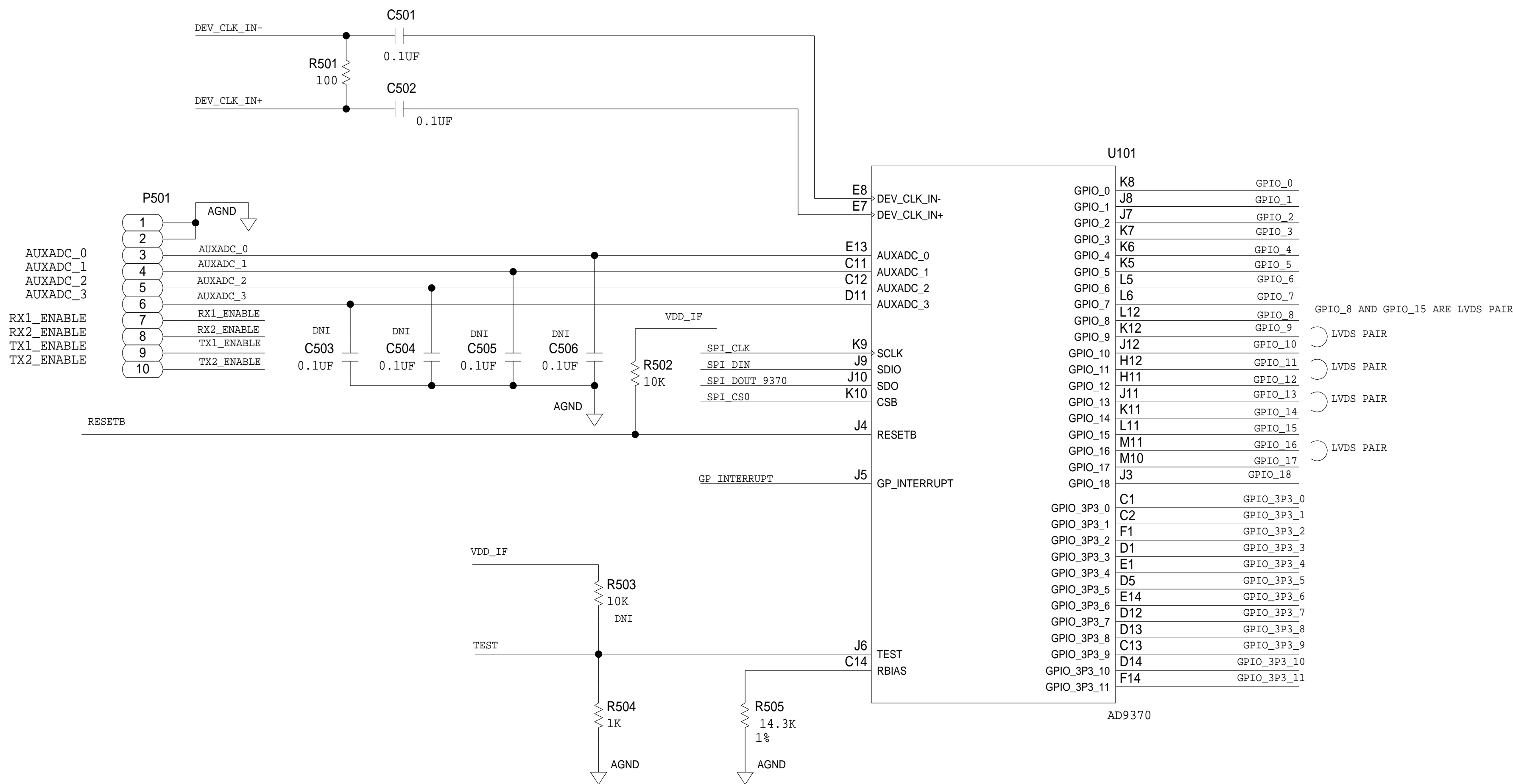
FOOTPRINTS OVERLAP IN LAYOUT
FOR CRYSTAL PACKAGE OPTION

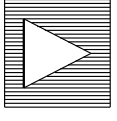


JESD INTERFACE / GPIO / JTAG

REVISIONS

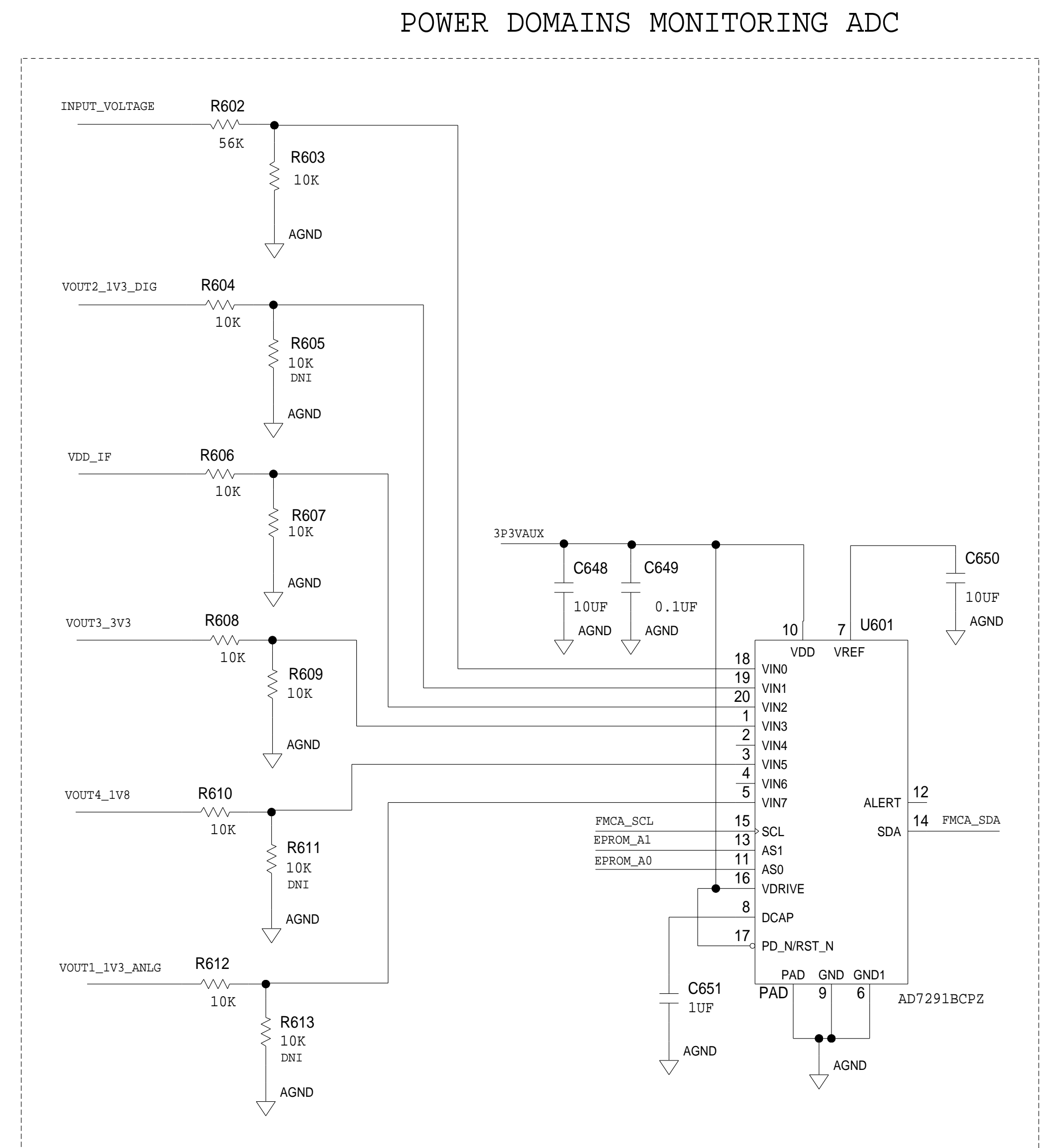
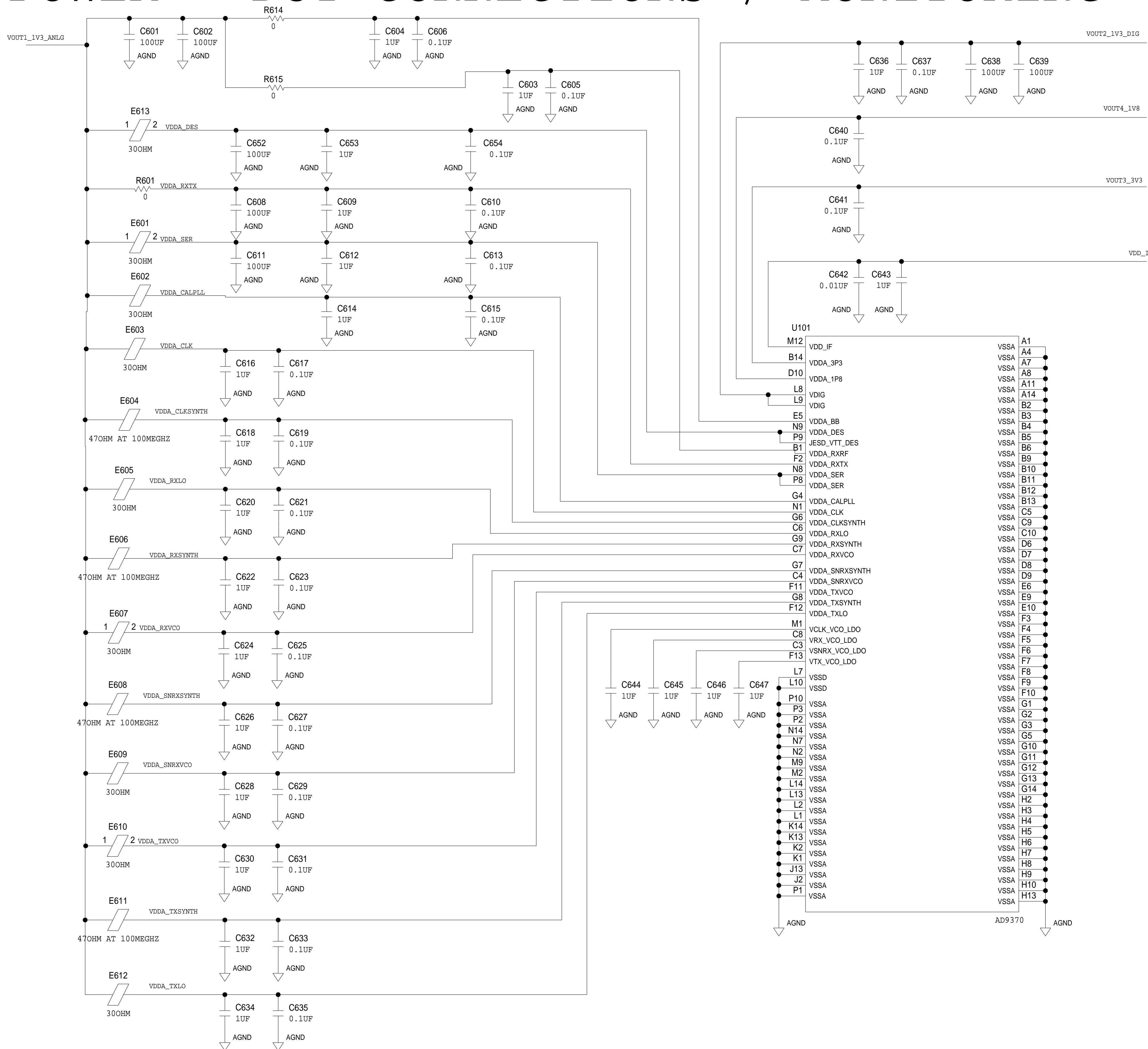
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s): AD9371		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042572		REV B
	PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1
SHEET 5 OF 8			

POWER - DUT CONNECTIONS / MONITORING

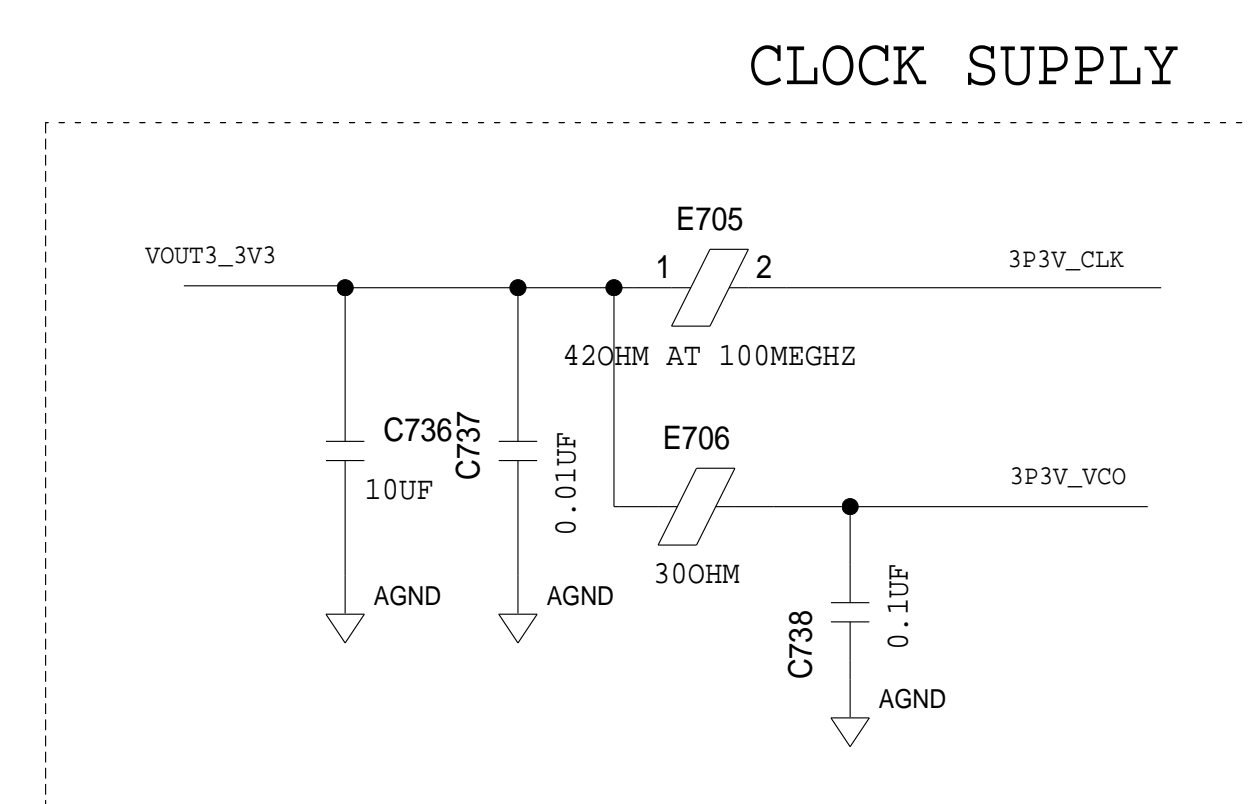
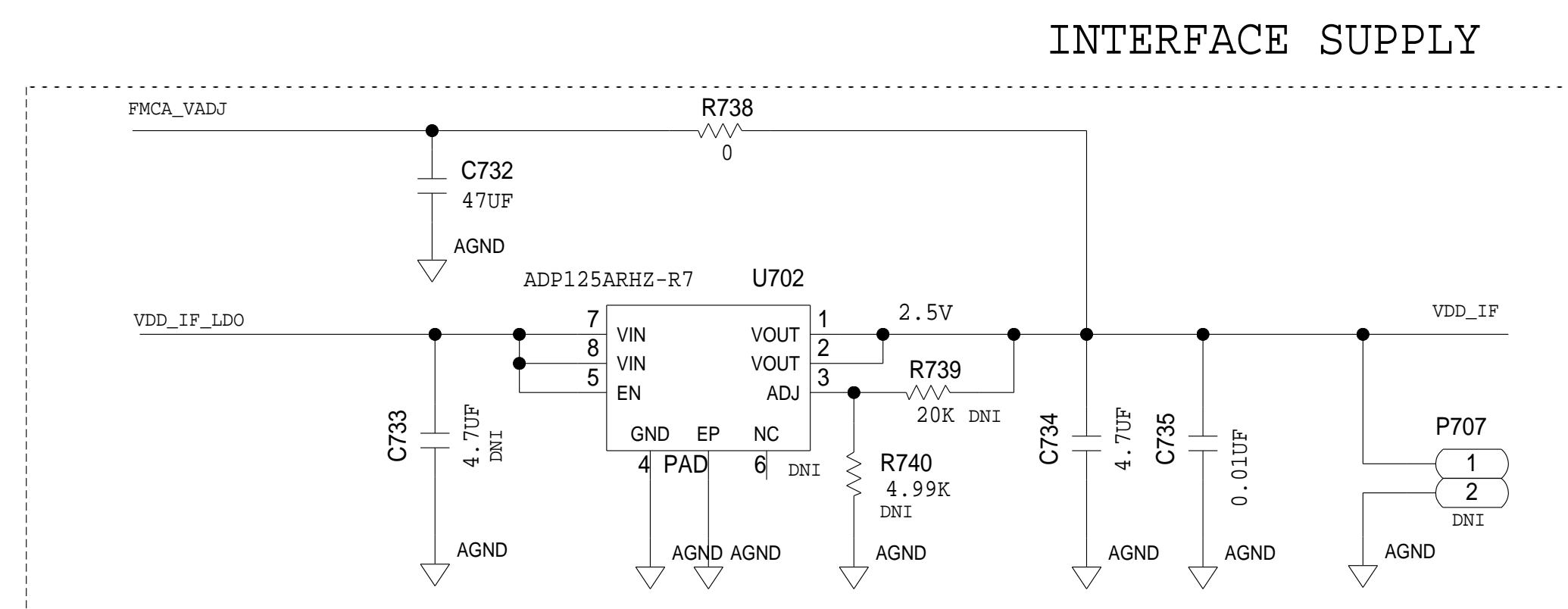
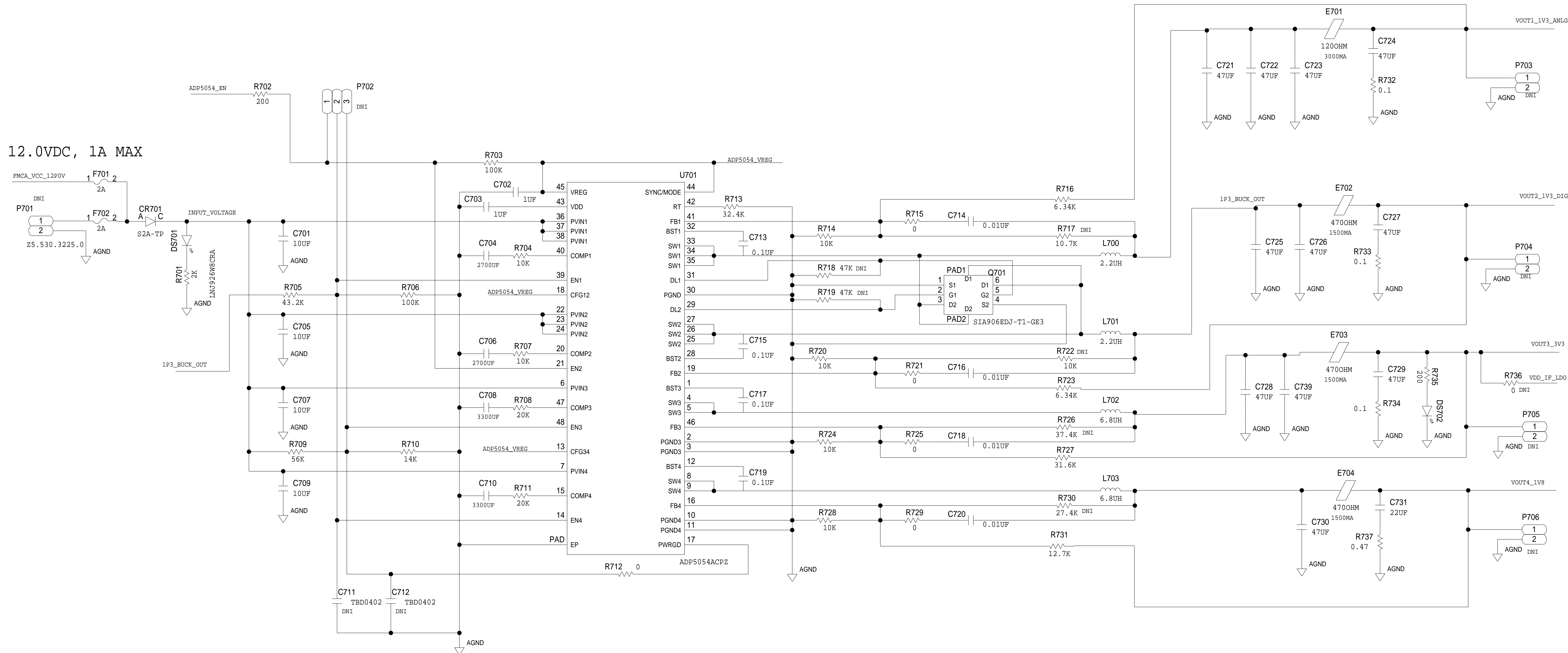
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED




SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042572	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 6 OF 8

POWER SUPPLY

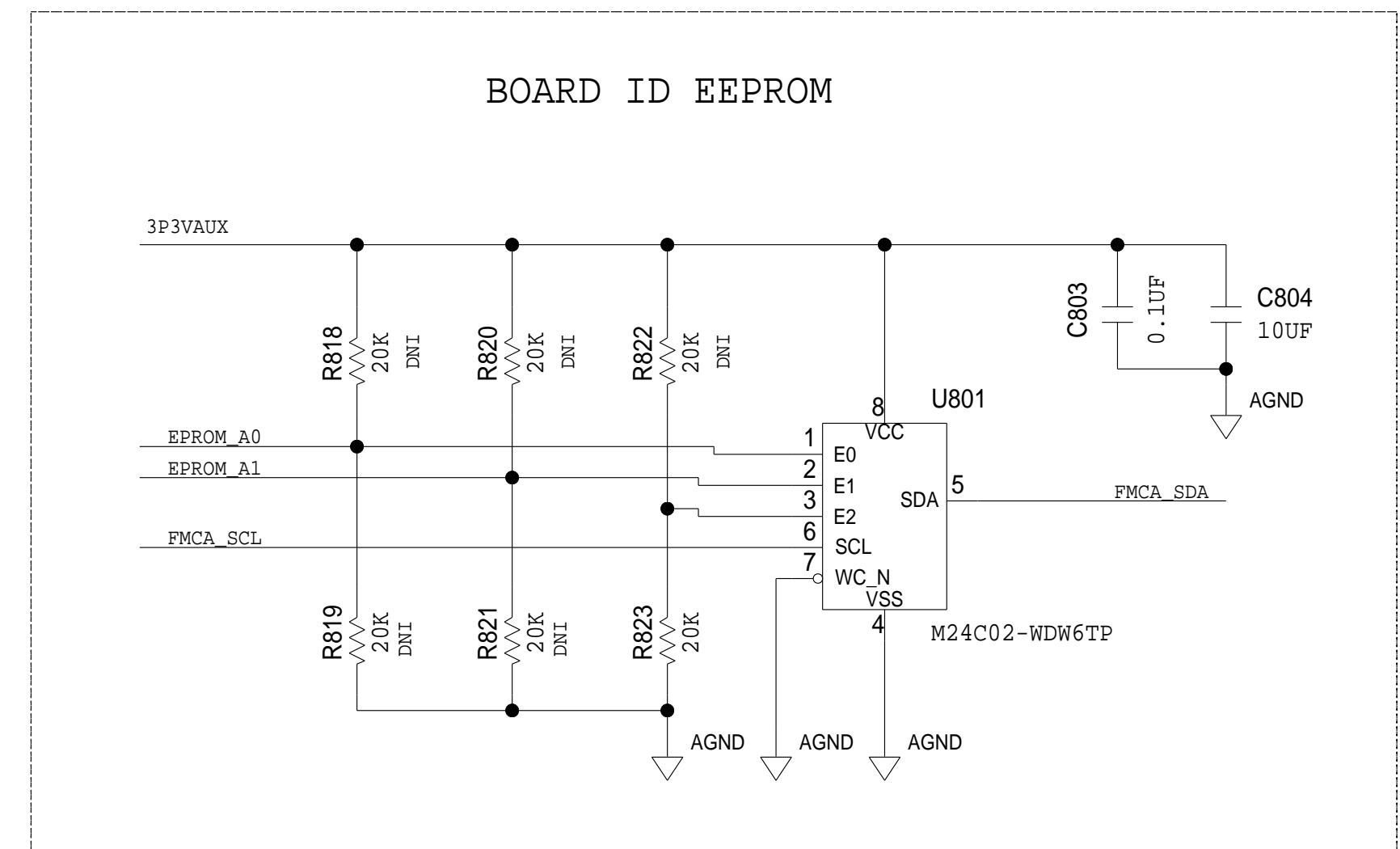
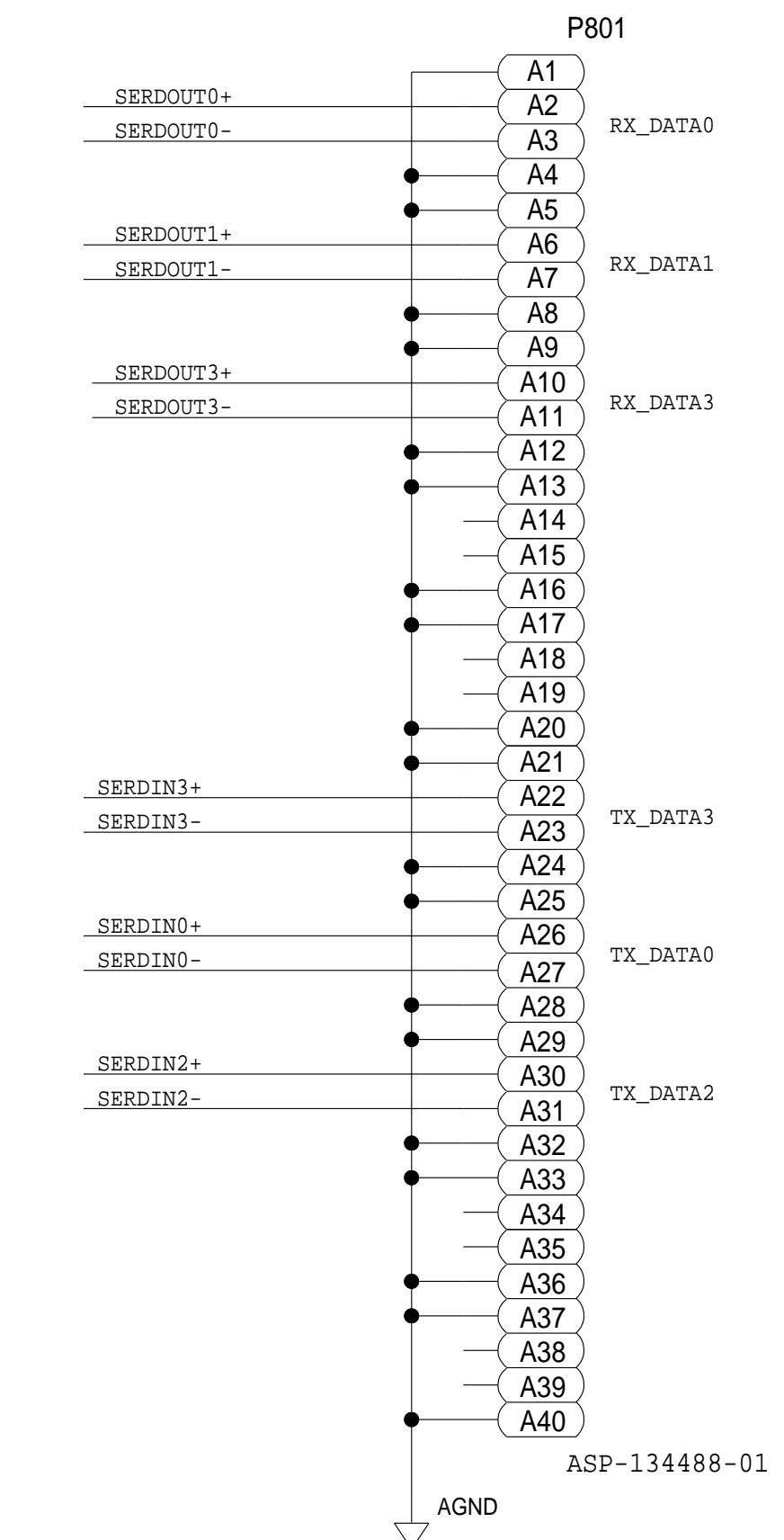
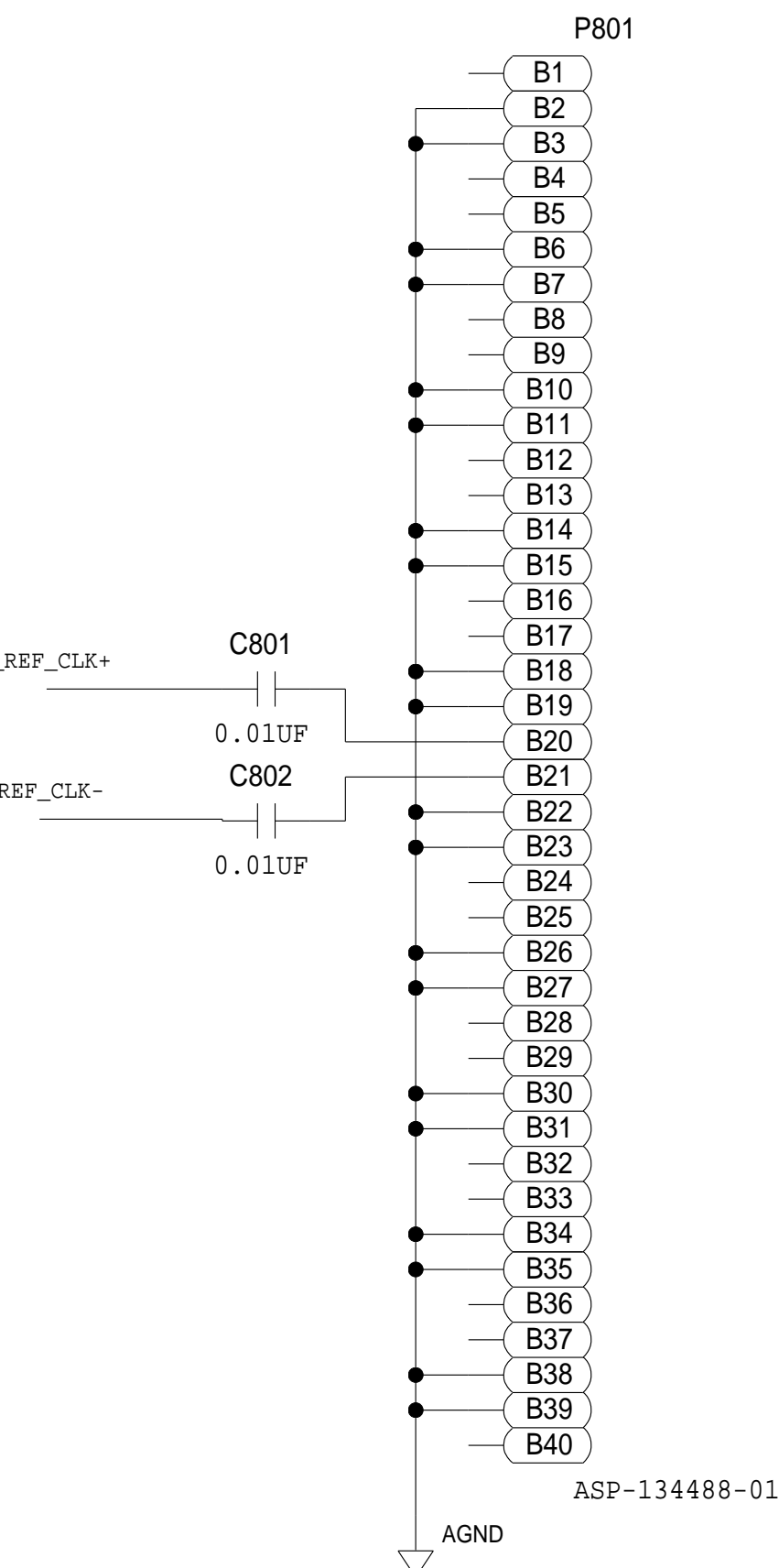
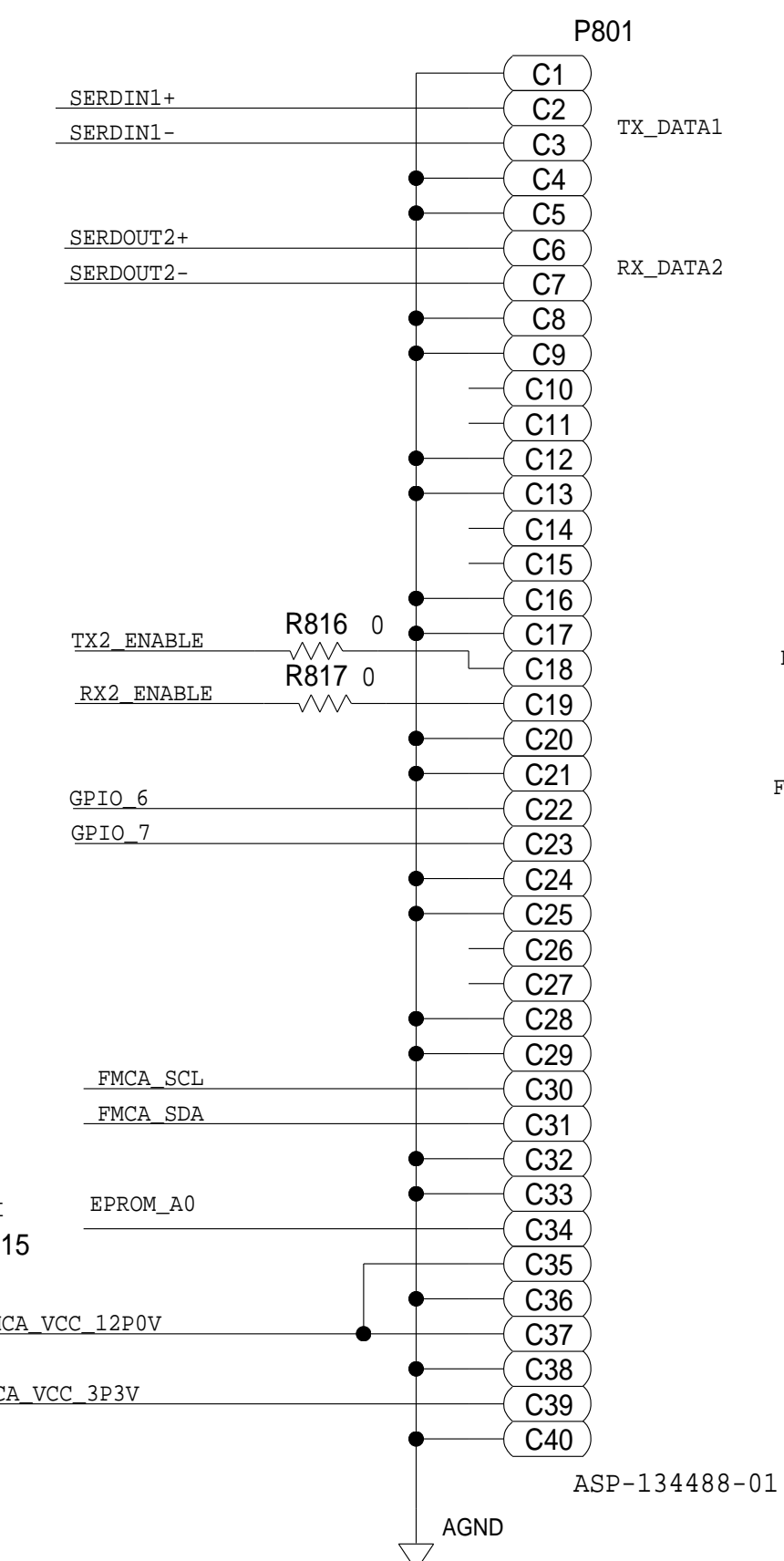
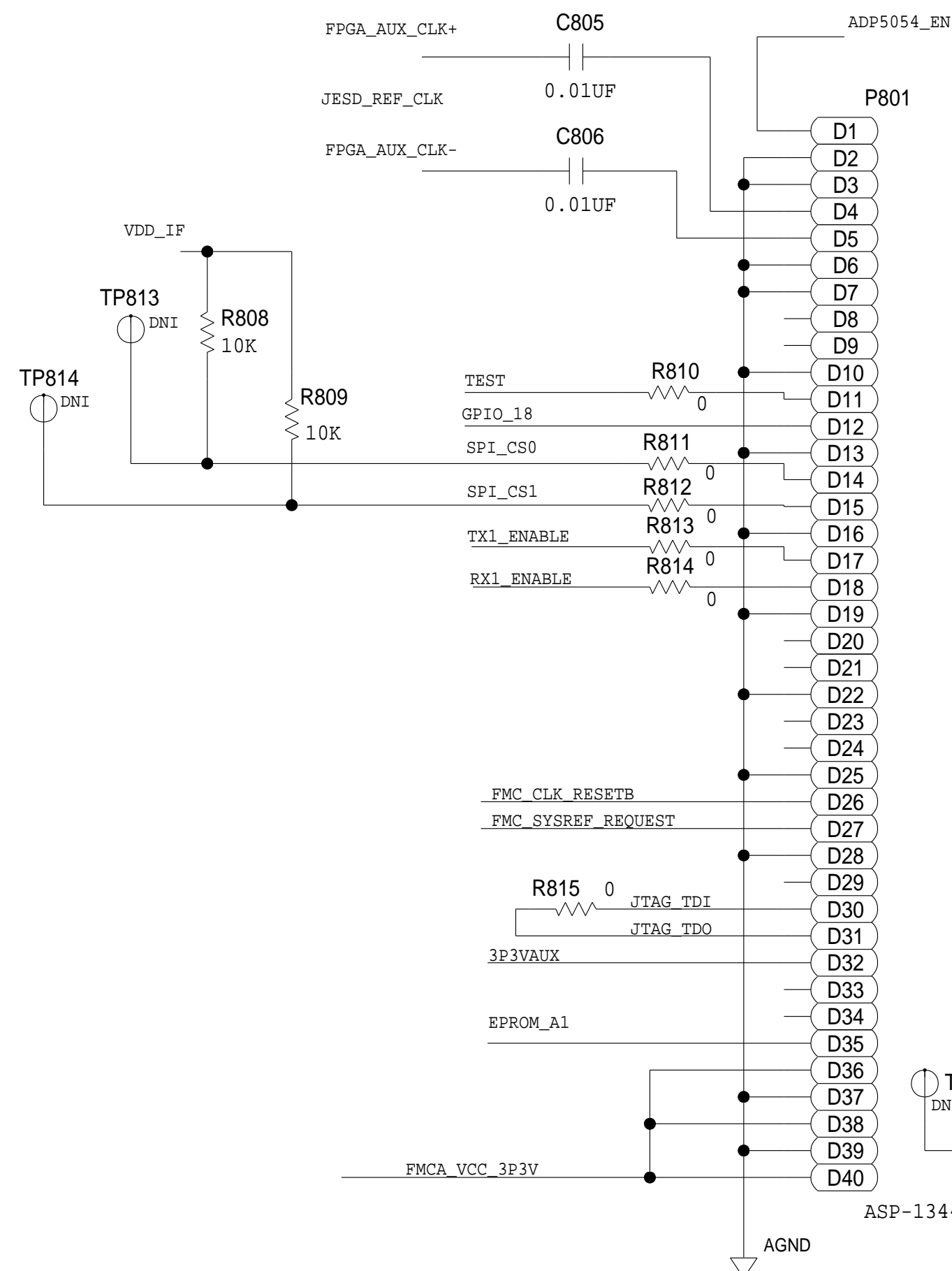
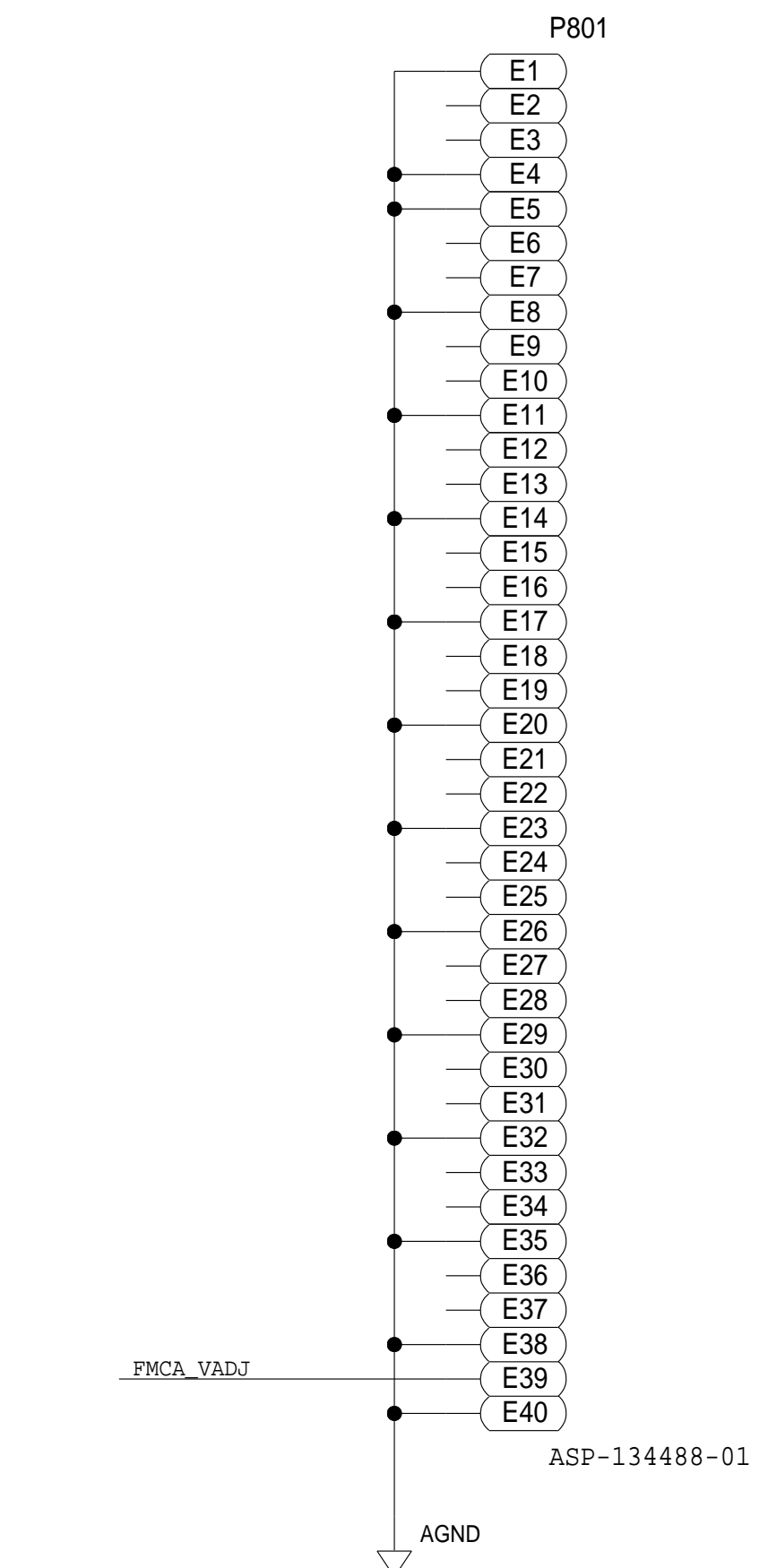
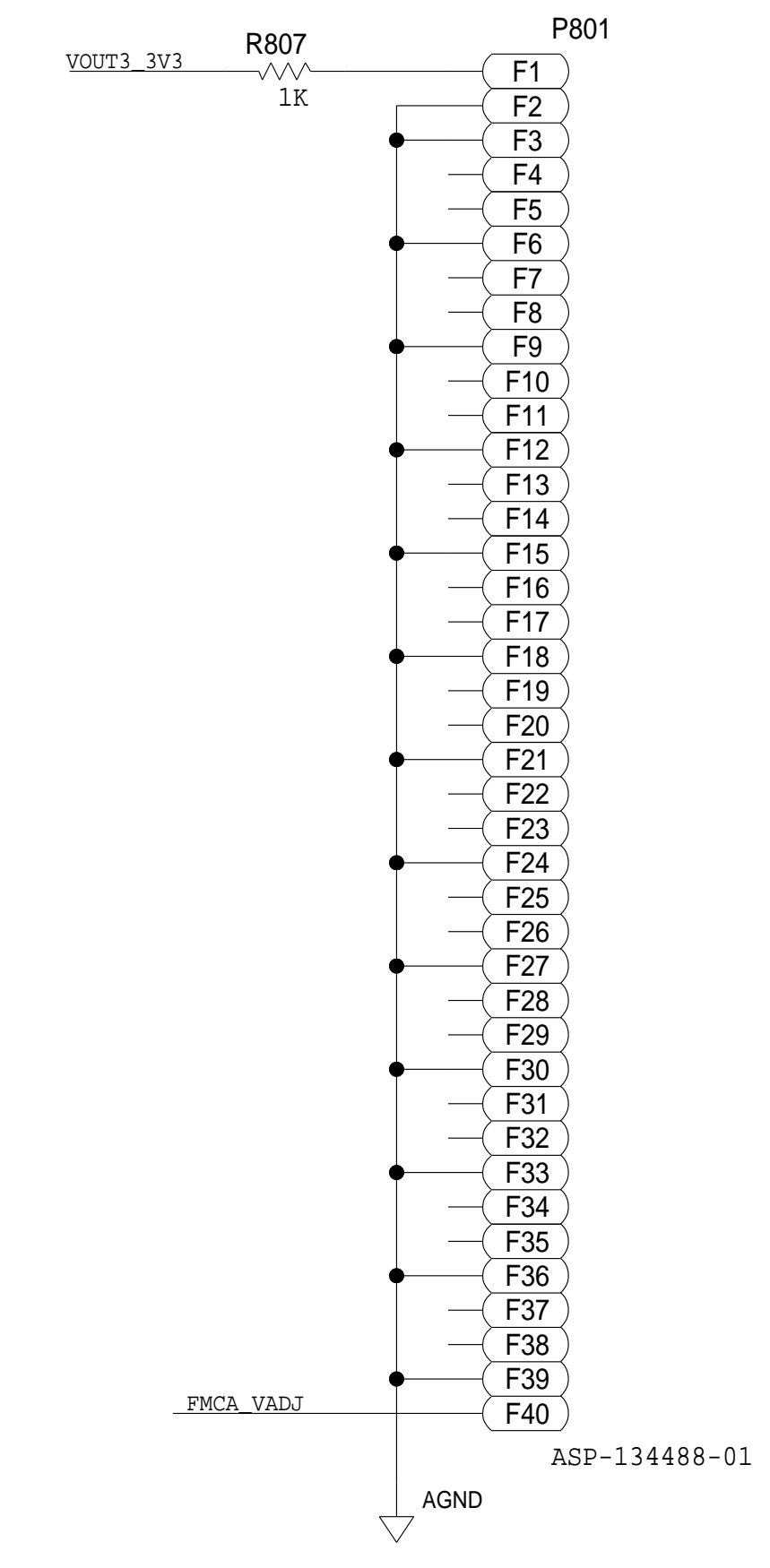
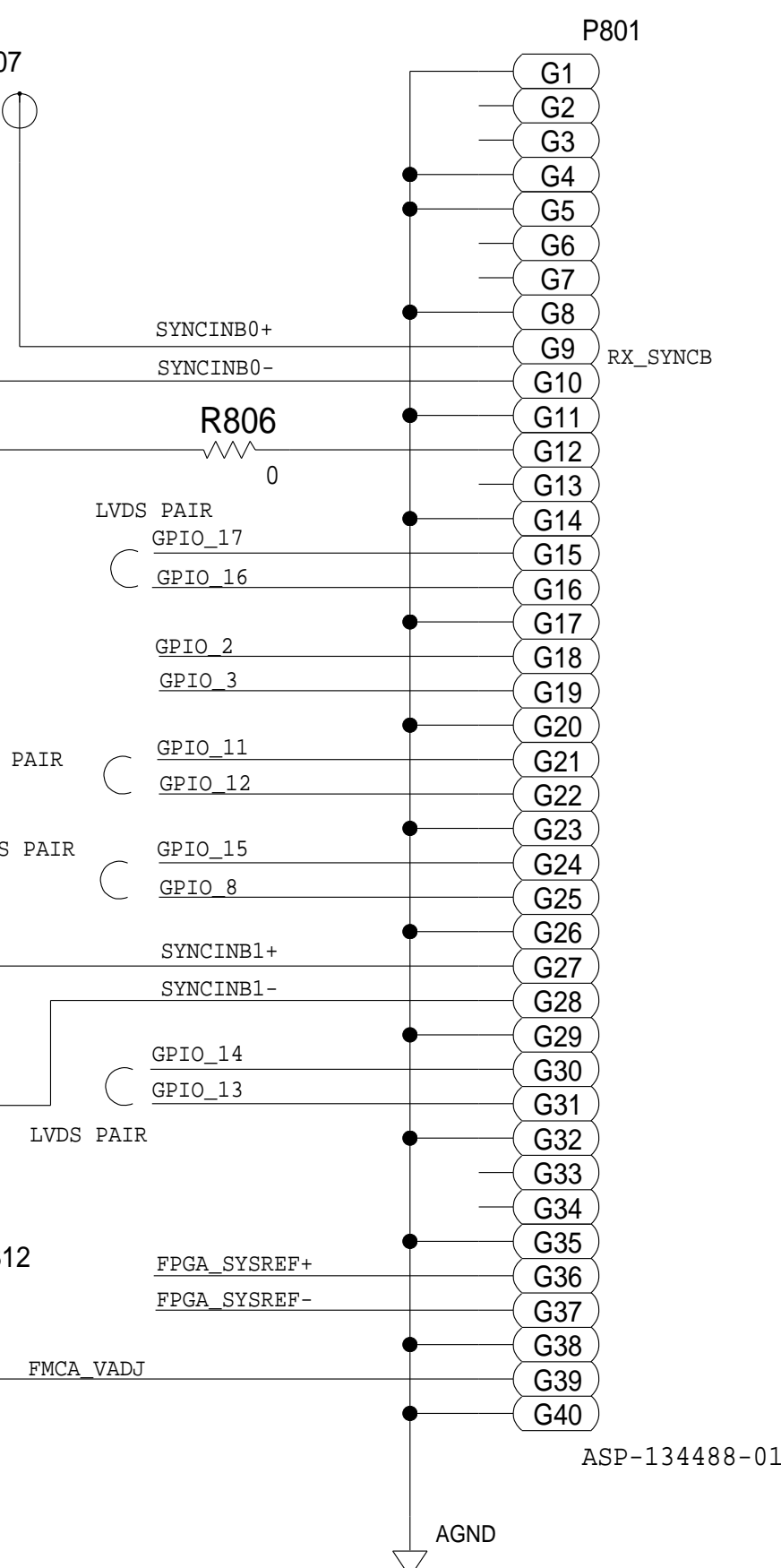
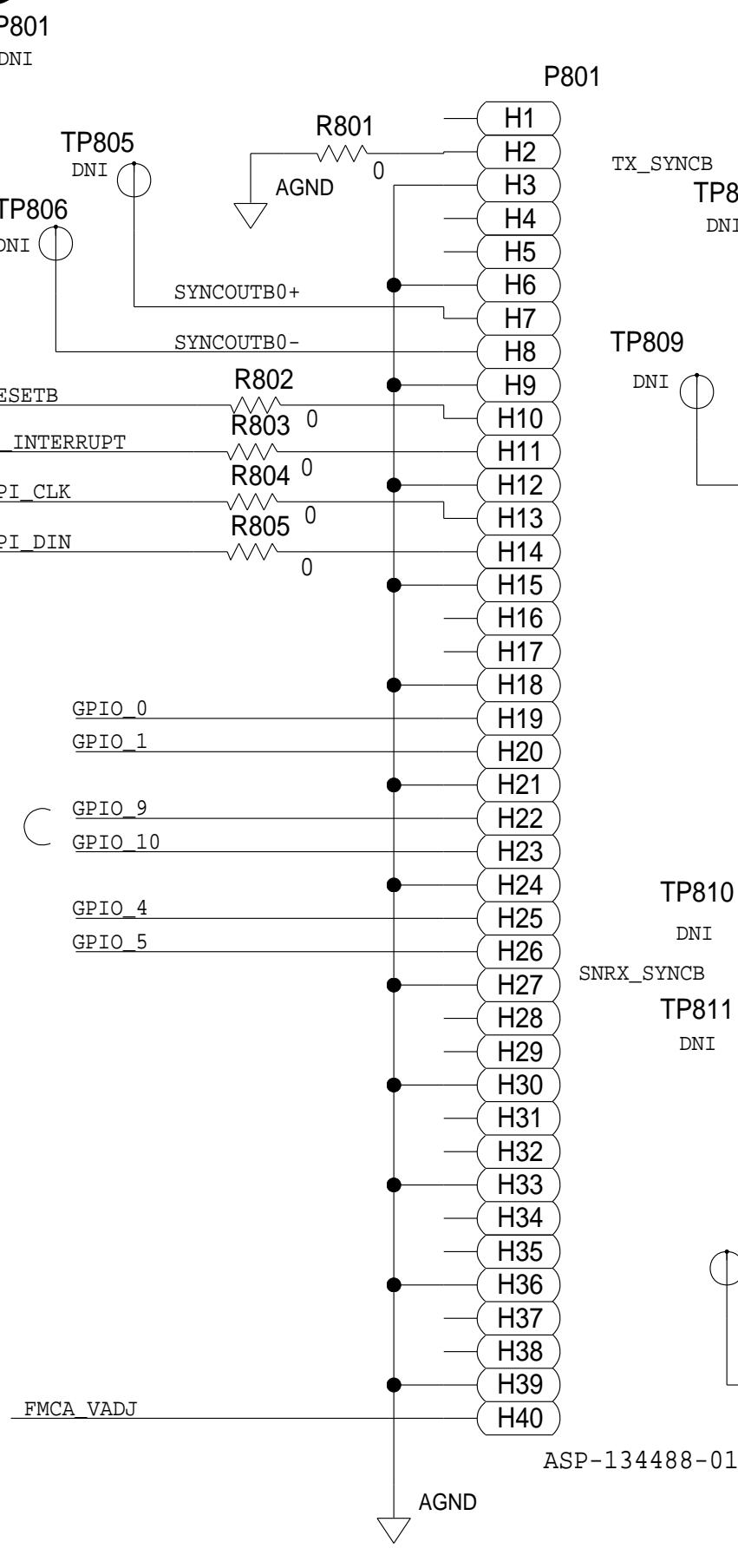
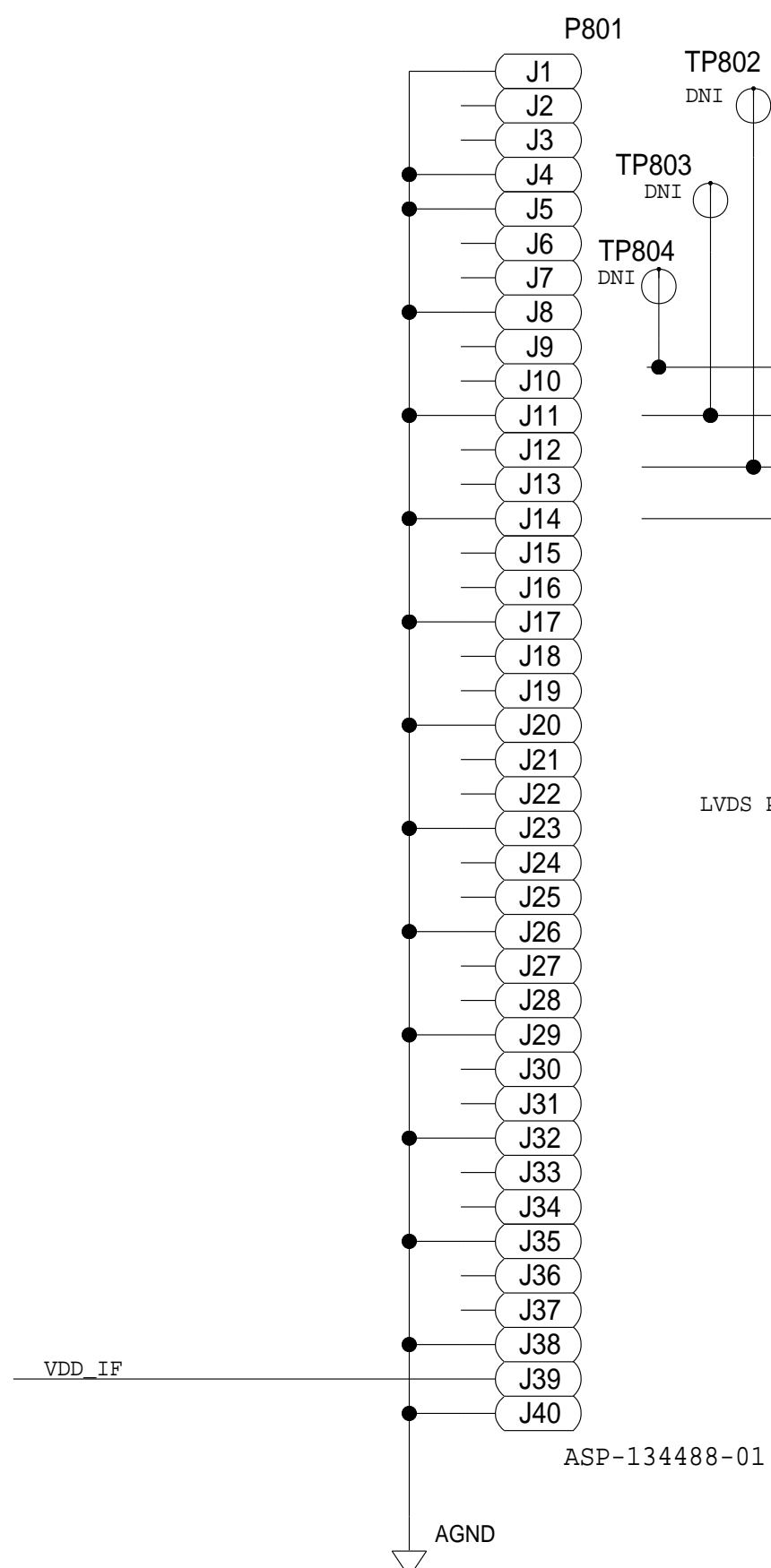
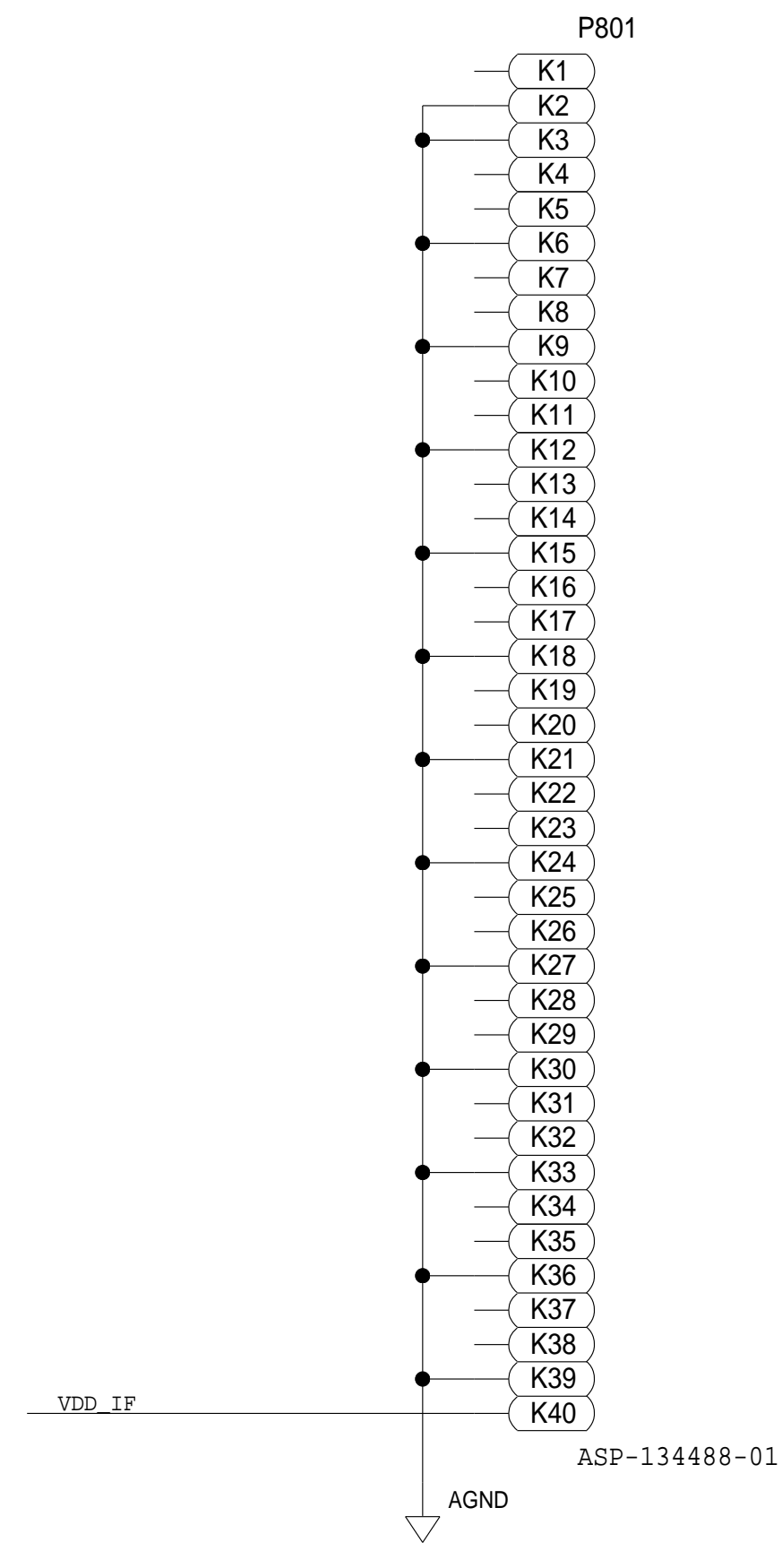
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 ANALOG DEVICES	<h1 style="margin: 0;">SCHEMATIC</h1>			
	HW TYPE : Customer Evaluation Product(s) : AD9371			
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	PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 7 OF 8

FMC – FPGA CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042572	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 8 OF 8